VT8235

V-Link Client
Highly Integrated
South Bridge

High Bandwidth V-Link Client Controller
Integrated Fast Ethernet
Integrated Direct Sound AC97 Audio,
UltraDMA-133/100/66/33 Master Mode EIDE Controller,
Six Port USB Controller for USB 2.0 and USB 1.1,
Keyboard / Mouse Controller, RTC
LPC, SMBus, Serial IRQ, Plug and Play, ACPI,
and PC2001 Compliant Enhanced Power Management

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VIA TECHNOLOGIES, INC.

Copyright Notice:

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Offices:

USA Office:
940 Mission Court
Fremont, CA 94539
USA
Tel: (510) 683-3300
Fax: (510) 683-3301 or (510) 687-4654
Web: http://www.viatech.com

Taipei Office:
8th Floor, No. 533
Chung-Cheng Road, Hsin-Tien
Taipei, Taiwan ROC
Tel: (886-2) 2218-5452
Fax: (886-2) 2218-5453
Web: http://www.via.com.tw

REVISION HISTORY

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1.1	9/12/02	Updated VIA Corporate Logo on cover page; Updated V-Link feature bullets Fixed misc typos and document formatting inconsistencies Fixed Device #'s in register summary table headings Fixed notes under Port 71 and 75 register descriptions Fixed Dev17 F0 Rx5B[2], 81[2], 82[6]; Updated marking specs Fixed VBAT voltage spec; Removed VPDVREF & VSDVREF from elec spec tables	DH
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VT8235

LOW COST V-LINK CLIENT
HIGHLY INTEGRATED SOUTH BRIDGE

HIGH BANDWIDTH V-LINK CLIENT CONTROLLER
INTEGRATED FAST ETHERNET,
INTEGRATED DIRECT SOUND AC97 AUDIO,
ULTRADMA-133/100/66/33 MASTER MODE EIDE CONTROLLER,
SIX PORT USB 2.0 CONTROLLER, KEYBOARD / MOUSE CONTROLLER,
RTC, LPC, SMBUS, SERIAL IRQ, PLUG AND PLAY, ACPI,
AND PC2001 COMPLIANT ENHANCED POWER MANAGEMENT

PRODUCT FEATURES

- **Inter-operable with VIA Host-to-V-Link Host Controller**
  - Combine with VT8754 (Apollo P4X333) for a complete 533 / 400 MHz FSB Pentium 4 system
  - Combine with VT8377 (Apollo KX400) for a complete 266 / 200 MHz FSB Athlon Socket-A system

- **High Bandwidth 533 MB/s 8-bit V-Link Client Controller**
  - Supports 66 MHz V-Link Client interface with total bandwidth of 533 MB/sec
  - V-Link operates in 2x, 4x, and 8x modes
  - Full duplex commands with separate Strobe / Command
  - Request / Data split transaction
  - Configurable outstanding transaction queue for V-Link Client accesses
  - Auto Client Retry to eliminate V-Link Host-Client Retry cycles
  - Intelligent V-Link transaction protocol to eliminate data wait-state / throttle transfer latency; all V-Link transactions for both Host and Client have a consistent view of transaction data depth and buffer size to avoid data overflow.
  - Highly efficient V-Link arbitration with minimum overhead; all V-Link transactions have predictable cycle length with known Command / Data duration
  - Auto connect / reconnect capability and dynamic stop for minimum power consumption
  - Parity checking to insure correct data transfers

- **Integrated Peripheral Controllers**
  - Integrated Fast Ethernet Controller with 1 / 10 / 100 Mbit capability
  - Integrated USB 2.0 Controller with three root hubs and six function ports
  - Dual channel UltraDMA-133 / 100 / 66 / 33 master mode EIDE controller
  - AC-link interface for AC-97 audio codec and modem codec
  - HSP modem support
  - Integrated DirectSound compatible digital audio controller
  - LPC interface for Low Pin Count interface to Super-I/O or ROM

- **Integrated Legacy Functions**
  - Integrated Keyboard Controller with PS2 mouse support
  - Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM and Day/Month Alarm for ACPI
  - Integrated DMA, timer, and interrupt controller
  - Serial IRQ for docking and non-docking applications
  - Fast reset and Gate A20 operation

- **Concurrent PCI Bus Controller**
  - 33 MHz operation
  - Supports up to six PCI masters
  - Peer concurrency
  - Concurrent multiple PCI master transactions; i.e., allow PCI masters from both PCI buses active at the same time
  - Zero wait state PCI master and slave burst transfer rate
  - PCI to system memory data streaming up to 132Mbyte/sec (data sent to north bridge via high speed V-Link Interface)
  - PCI master snoop ahead and snoop filtering
  - Eight DW of CPU to PCI posted write buffers
  - Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
  - Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
  - Four lines of post write buffers from PCI masters to DRAM
  - Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
  - Delay transaction from PCI master accessing DRAM
  - Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks)
  - Symmetric arbitration between Host/PCI bus for optimized system performance
  - Complete steerable PCI interrupts
  - PCI-2.2 compliant, 32 bit 3.3V PCI interface with 5V tolerant inputs

- **Fast Ethernet Controller**
  - High performance PCI master interface with scatter / gather and bursting capability
  - Standard MII interface to external PHYceiver
  - 1 / 10 / 100 MHz full and half duplex operation
  - Independent 2K byte FIFOs for receive and transmit
  - Flexible dynamically loadable EEPROM algorithm
  - Physical, Broadcast, and Multicast address filtering using hashing function
  - Magic packet and wake-on-address filtering
  - Software controllable power down

- **UltraDMA-133 / 100 / 66 / 33 Master Mode EIDE Controller**
  - Dual channel master mode hard disk controller supporting four Enhanced IDE devices
  - Transfer rate up to 133MB/sec to cover PIO mode 4, multi-word DMA mode 2 drives, and UltraDMA-133 interface
  - Increased reliability using UltraDMA-133/100/66 transfer protocols
  - Thirty-two levels (doublewords) of prefetch and write buffers
  - Dual DMA engine for concurrent dual channel operation
  - Bus master programming interface for SFF-8038i rev.1.0 and Windows-95 compliant
  - Full scatter gather capability
  - Support ATAPI compliant devices including DVD devices
  - Support PCI native and ATA compatibility modes
  - Complete software driver support

- **Direct Sound Ready AC97 Digital Audio Controller**
  - AC-Link access to 4 CODECs (AC97 + AMC97 + MC97)
  - Multichannel Audio
  - Bus Master Scatter / Gather DMA
  - Dedicated read and write channels supporting simultaneous stereo playback and record
  - Dedicated read and write channels supporting simultaneous modem receive and transmit
  - 1 stereo DirectSound channel with source / volume control / mixer
  - 1 shared FM / SPDIF PCM read channel
  - 1 dedicated channel supporting multi-channel audio
  - 32-byte line-bufers for each SGD channel
  - Programmable 8bit / 16bit mono / stereo PCM data format support
  - AC97 2.1 compliant

- **System Management Bus Interface**
  - Host interface for processor communications
  - Slave interface for external SMBus masters

- **Universal Serial Bus Controller**
  - USB v2.0 and Enhanced Host Controller Interface (EHCI) v1.0 compatible
  - USB v1.1 and Universal Host Controller Interface (UHCI) v1.1 compatible
  - Eighteen level (doublewords) data FIFO with full scatter and gather capability
  - Three root hubs and six function ports
  - Integrated physical layer transceivers with optional over-current detection status on USB inputs
  - Legacy keyboard and PS/2 mouse support

- **Sophisticated PC2001-Compatible Mobile Power Management**
  - Supports both ACPI (Advanced Configuration and Power Interface) and legacy (APM) power management
  - ACPI v1.0 Compliant
  - APM v1.2 Compliant
  - CPU clock throttling and clock stop control for complete ACPI C0 to C3 state support
  - PCI bus clock run, Power Management Enable (PME) control, and PCI/CPU clock generator stop control
  - Supports multiple system suspend types: power-on suspends with flexible CPU/PCI bus reset options, suspend to DRAM, and suspend to disk (soft-off), all with hardware automatic wake-up
  - Multiple suspend power plane controls and suspend status indicators
  - One idle timer, one peripheral timer and one general purpose timer, plus 24/32-bit ACPI compliant timer
  - Normal, doze, sleep, suspend and conserve modes
  - Global and local device power control
  - System event monitoring with two event classes
  - Primary and secondary interrupt differentiation for individual channels
  - Dedicated input pins for power and sleep buttons, external modem ring indicator, and notebook lid open/close for system wake-up
  - 32 general purpose input ports and 32 output ports
  - Multiple internal and external SMI sources for flexible power management models
  - Enhanced integrated real time clock (RTC) with date alarm, month alarm, and century field
  - Thermal alarm on external temperature sensing circuit
  - I/O pad leakage control

- **Plug and Play Controller**
  - PCI interrupts steerable to any interrupt channel
  - Steerable interrupts for integrated peripheral controllers: USB, floppy, serial, parallel, and audio
  - Microsoft Windows XP™, Windows NT™, Windows 2000™, Windows 98™ and plug and play BIOS compliant

- **Built-in NAND-tree pin scan test capability**

- **0.22um, 2.5V, low power CMOS process**

- **Single chip 27 x 27 mm, 1.0 mm ball pitch, 487 pin BGA**

OVERVIEW

The VT8235 South Bridge is a high integration, high performance, power-efficient, and high compatibility device that supports Intel and non-Intel based processor to V-Link bus bridge functionality to make a complete Microsoft PC2001-compliant PCI/LPC system. The VT8235 includes standard intelligent peripheral controllers:

a) IEEE 802.3 compliant 10 / 100 Mbps PCI bus master Ethernet MAC with standard MII interface to external PHYceiver.

b) Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands. Dedicated FIFO coupled with scatter and gather master mode operation allows high performance transfers between PCI and IDE devices. In addition to standard PIO and DMA mode operation, the VT8235 also supports the UltraDMA-133, 100, 66, and 33 standards to allow reliable data transfer at rates up to 133 MB/sec. The IDE controller is SFF-8038i v1.0 and Microsoft Windows-family compliant.

c) Universal Serial Bus controller that is USB v2.0 / 1.1 and Universal HCI v2.0 / 1.1 compliant. The VT8235 includes three root hubs with six function ports with integrated physical layer transceivers. The USB controller allows hot plug and play and isochronous peripherals to be inserted into the system with universal driver support. The controller also implements legacy keyboard and mouse support so that legacy software can run transparently in a non-USB-aware operating system environment.

d) Keyboard controller with PS2 mouse support.

e) Real Time Clock with 256 byte extended CMOS. In addition to the standard ISA RTC functionality, the integrated RTC also includes the date alarm, century field, and other enhancements for compatibility with the ACPI standard.

f) Notebook-class power management functionality compliant with ACPI and legacy APM requirements. Multiple sleep states (power-on suspend, suspend-to-DRAM, and suspend-to-Disk) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling and stop (Intel processor protocol), PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.

g) Full System Management Bus (SMBus) interface.

h) Integrated bus-mastering dual full-duplex direct-sound AC97-link-compatible sound system.

i) Plug and Play controller that allows complete steerability of all PCI interrupts and internal interrupts / DMA channels to any interrupt channel. One additional steerable interrupt channel is provided to allow plug and play and reconfigurability of on-board peripherals for Windows family compliance.

The VT8235 also enhances the functionality of the standard ISA peripherals. The integrated interrupt controller supports both edge and level triggered interrupts channel by channel. The integrated DMA controller supports type F DMA in addition to standard ISA DMA modes. Compliant with the PCI-2.2 specification, the VT8235 supports delayed transactions and remote power management so that slower ISA peripherals do not block the traffic of the PCI bus. Special circuitry is built in to allow concurrent operation without causing dead lock even in a PCI-to-PCI bridge environment. The chip also includes eight levels (doublewords) of line buffers from the PCI bus to the ISA bus to further enhance overall system performance.

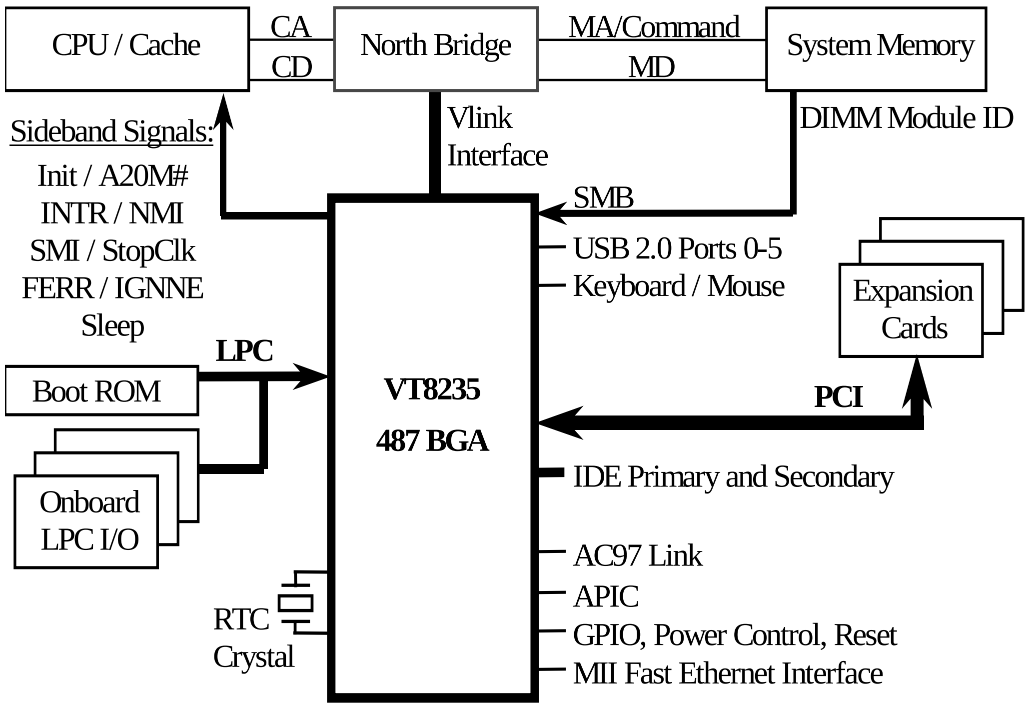


Figure 1. PC System Configuration Using the VT8235

PINOUTS

Figure 2. VT8235 Ball Diagram (Top View)

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	GND	GND	T RDY#	CBE 2#	AD17	GPIO 11	GPIO 12	AGP BZ#	MRX D3	MRX ERR	MTX D1	MTX CLK	EE CS#	EE DO	USB OC0#	USB GND	USB P4+	USB GND	USB P2+	USB GND	USB P0+	USB GND	VCC UPLL	USB VCC	USB VCC	USB VCC
B	GND	GND	DEV SEL#	FRM#	AD16	AD19	GPIO 9	GPIO 13	MD IO	MRX CLK	MTX D2	MTX ENA	M CRS	EE DI	USB OC1#	USB GND	USB P4–	USB GND	USB P2–	USB GND	USB P0–	USB GND	GND UPLL	USB VCC	USB VCC	USB VCC
C	SERR#	PERR#	STOP#	I RDY#	REQ 1#	AD18	GPIO 15	VGATE GPIO8	MD CK	MRX DV	MTX D3	MTX D0	M COL	EE CK	USB OC2#	USB GND	USB GND	USB GND	USB GND	USB GND	USB GND	USB GND	USB REXT	USB VCC	USB VCC	USB VCC
D	CBE 1#	AD15	PAR	REQ 2#	GNT 1#	REQ 0#	GPIO 10	GPIO 14	MRX D2	MRX D1	MII VCC	MII VCC	MII VCC25	USB OC4#	VSUS USB	USB GND	USB P5–	USB GND	USB P3–	USB GND	USB P1–	VCC UPLL	USB CLK	USB VCC	VAD 8	V PAR
E	AD11	AD13	AD14	GNT 2#	VCC 33	GNT 0#	RAM VCC	RAM GND	GND	MRX D0	MII VCC	MII VCC	MII VCC25	USB OC5#	USB OC3#	GND	USB P5+	USB GND	USB P3+	USB GND	USB P1+	GND UPLL	GND	VAD 5	GND	VAD 4
F	AD10	AD9	AD12	CBE 0#	VCC 33	GND	VCC 33	VCC 33	VCC	VCC	GND	VCC 33	VCC 33	VCC	VCC	VCC 33	VCC 33	USB GND	USB GND	USB GND	USB GND	VCC VK	VAD 9	VBE 0#	VAD 0	VAD 1
G	AD7	AD6	AD4	AD8	GND	G6	7	8	9	10	11	12	13	14	15	16	17	18	19	G20	VCC VK	VAD 11	VAD 10	VAD 13	DN STB	DN STB#
H	AD5	AD2	AD0	REQ 3#	VCC	H	GPIO	Pins			LAN	Pins					USB	Pins		H	VCC VK	VAD 12	GND	UP STB	GND	UP STB#
J	AD3	AD1	AD21	GNT 3#	VCC	J														J	VCC	VAD 14	VL VREF	DN CMD	VAD 3	VAD 2
K	AD20	AD22	AD23	GND	VCC	K					K11	12	13	14	15	K16			V-Link	K	VCC	VAD 15	VL COMP	VAD 6	UP CMD	VAD 7
L	CBE 3#	AD24	AD25	REQ 4#	VCC 33	L	PCI	Pins		L10	GND	GND	GND	GND	GND	GND	L17		Pins	L	VCC VK	VCC VK	GND	V CLK	GND	VBE 1#
M	AD27	AD26	AD28	GNT 4#	VCC 33	M				M	GND	GND	GND	GND	GND	GND	M			M	VCC VK	VCC VK	VCC VK	VCC VK	VCC VK	VCC VK
N	AD29	AD31	AD30	REQ5# GPI7	GND	N				N	GND	GND	GND	GND	GND	GND	N			N	VCC VK	VCC VK	VCC VK	VCC VK	VCC VK	VCC VK
P	INT A#	INT B#	INT C#	GNT5# GPO7	VCC 33	P				P	GND	GND	GND	GND	GND	GND	P			P	VCC 33	PLL VCC	PLL GND	VRD SLP	VID SEL	DP SLP#
R	INT D#	PCI RST#	AC RST#	GND	VCC 33	R				R	GND	GND	GND	GND	GND	GND	R		CPU	R	VCC 33	PCI CLK	NMI	GHI#	INIT#	STP CLK#
T	AC SYNC	AC SDI0	AC BTCK	VSUS 25	VCC	T	AC97	Pins		T10	GND	GND	GND	GND	GND	GND	T17		Pins	T	VCC	APIC D0	INTR	SMI#	A20M#	IGN NE#
U	AC SDO	AC SDI2	AC SDI1	VSUS 25	VCC	U					U11	12	13	14	15	U16				U	VCC	VCC	APIC CLK	TPO	SLP#	FERR#
V	AC SDI3	KB DT	KB CK	GND	VCC	V	KB/MS	Pins											Pri	V	GND	GND	APIC D1	PD CS1#	PD A1	PD A2
W	MS DT	MS CK	PME#	BAT LOW#	VCC 33	W	PM	Pins											IDE	W	GND	PD VREF	PD COMP	PD CS3#	GND	PD DAK#
Y	CPU MISS	RING#	SUS ST#	THRM#	VCC 33	Y	LPC	Pins			X-Bus	Pins			Sec	IDE	Pins		Pins	Y	VCC 33	PD DRQ	PD A0	PD IOR#	PD IOW#	PD RDY
AA	EXT SMI#	SUS A#	GPO 0	VSUS 33	GND	AA6	7	8	9	10	11	12	13	14	15	16	17	18	19	AA20	VCC 33	PD D15	GND	PD D0	PD D1	PD D14
AB	SUS CLK	SMB ALRT#	SMB CK1	VSUS 33	GND	VCC 33	VCC 33	VCC	VCC	VCC 33	VCC 33	GND	GND	VCC 33	VCC 33	VCC	VCC	GND	GND	VCC 33	VCC 33	GND	PD D12	PD D2	GND	PD D13
AC	LID#	SMB DT1	GPI 1	VSUS 33	VSUS 33	GPIO E	CPU STP#	GND	GND	IOR#	SA19 strap	OSC	XD 1	XD 0	SD COMP	GND	GND	VCC 33	VCC 33	GND	SD IOW#	SDA1 strap	SD CS1#	PD D4	PD D11	PD D3
AD	SMB DT2	PWR BTN#	IN TRUD#	RTC X1	RSM RST#	GPIO D	L REQ#	L AD2	IOW#	IO RDY#	SA18 strap	SOE# strap	XD 7	XD 4	SD RDY	SDD1 SA01	SD VREF	SDD5 SA05	SDD9 SA09	SDD10 SA10	SDD13 SA13	SD DAK#	SDCS3# strap	PD D9	PD D5	PD D10
AE	SMB CK2	PWR OK#	GPI 0	V BAT	GPIO A	GPIO C	L FRM#	L AD1	SPKR strap	SER IRQ	SA17 strap	MEM R#	XD 6	XD 3	SD DRQ	GND	SDD4 SA04	SDD7 SA07	GND	SDD12 SA12	SDD15 SA15	GND	SDA0 strap	IRQ 14	GND	PD D6
AF	SUS C#	SUS B#	RTC X2	PWR GD	PCK RUN#	PCI STP#	L AD3	L AD0	TEST	MEM W#	SA16 strap	ROMCS #/strap	XD 5	XD 2	SDD0 SA00	SDD2 SA02	SDD3 SA03	SDD6 SA06	SDD8 SA08	SDD11 SA11	SDD14 SA14	SD IOR#	SDA2 strap	IRQ 15	PD D7	PD D8

Table 1. VT8235 Pin List (Numerical Order)

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name
A01	**P**	**GND**	D01	IO	CBE1#	H26	O	UPSTB#	U23	I	APICCLK	AD04	I	RTCX1
A02	**P**	**GND**	D02	IO	AD15	J01	IO	AD03	U24	O	TPO	AD05	I	RSMRST#
A03	IO	TRDY#	D03	IO	PAR	J02	IO	AD01	U25	OD	SLP#	AD06	IO	GPIOD / 30
A04	IO	CBE2#	D04	I	REQ2#	J03	IO	AD21	U26	I	FERR#	AD07	IO	LREQ#
A05	IO	AD17	D05	O	GNT1#	J04	O	GNT3#	V01	I	ACSDI3 /IO21/PCS1# /SB#	AD08	IO	LAD2
A06	IO	GPIO11	D06	I	REQ0#	J22	IO	VAD14	V02	IO	KBDT / KBRC	AD09	IO	IOW#
A07	IO	GPIO12 / INTE# / PCGNTA	D07	IO	GPIO10	**J23**	**P**	**VLVREF**	V03	IO	KBCK / A20G	AD10	I	IORDY
A08	I	AGPBZ# / GPI6	D08	IO	GPIO14 / INTG#	J24	I	DNCMD	**V04**	**P**	**GND**	AD11	IO	SA18 / O18 / strap
A09	I	MRXD3	D09	I	MRXD2	J25	IO	VAD03	**V22**	**P**	**GND**	AD12	O	SOE# / strap
A10	I	MRXERR	D10	I	MRXD1	J26	IO	VAD02	V23	O	APICD1	AD13	IO	XD7
A11	O	MTXD1	**D11**	**P**	**MIIVCC**	K01	IO	AD20	V24	O	PDCS1#	AD14	IO	XD4
A12	I	MTXCLK	**D12**	**P**	**MIIVCC**	K02	IO	AD22	V25	O	PDA1	AD15	I	SDRDY
A13	O	EECS#	**D13**	**P**	**MIIVCC25**	K03	IO	AD23	V26	O	PDA2	AD16	IO	SDD01 / SA01
A14	O	EEDO	D14	I	USBOC4#	**K04**	**P**	**GND**	W01	IO	MSDT / IRQ12	**AD17**	**P**	**SDVREF**
A15	I	USBOC0#	**D15**	**P**	**VSUSUSB**	K22	IO	VAD15	W02	IO	MSCK / IRQ1	AD18	IO	SDD05 / SA05
A16	**P**	**USBGND**	**D16**	**P**	**USBGND**	**K23**	**I**	**VLCOMP**	W03	I	PME#	AD19	IO	SDD09 / SA09
A17	IO	USBP4+	D17	IO	USBP5–	K24	IO	VAD06	W04	I	BATLOW# / GPI5	AD20	IO	SDD10 / SA10
A18	**P**	**USBGND**	**D18**	**P**	**USBGND**	K25	O	UPCMD	**W22**	**P**	**PDVREF**	AD21	IO	SDD13 / SA13
A19	IO	USBP2+	D19	IO	USBP3–	K26	IO	VAD07	**W23**	**I**	**PDCOMP**	AD22	O	SDDACK#
A20	**P**	**USBGND**	**D20**	**P**	**USBGND**	L01	IO	CBE3#	W24	O	PDCS3#	AD23	O	SDCS3# / strap
A21	IO	USBP0+	D21	IO	USBP1–	L02	IO	AD24	**W25**	**P**	**GND**	AD24	IO	PDD09
A22	**P**	**USBGND**	**D22**	**P**	**VCCUPLL**	L03	IO	AD25	W26	O	PDDACK#	AD25	IO	PDD05
A23	**P**	**VCCUPLL**	D23	I	USBCLK	L04	I	REQ4#	Y01	I	CPUMISS / GPI17	AD26	IO	PDD10
A24	**P**	**USBVCC**	**D24**	**P**	**USBVCC**	**L22**	**P**	**VCCVK**	Y02	I	RING# / GPI3	AE01	IO	SMBCK2 /
A25	**P**	**USBVCC**	D25	IO	VAD08	**L23**	**P**	**GND**	Y03	O	SUSST1# / GPO3	AE02	O	PWROK#
A26	**P**	**USBVCC**	D26	IO	VPAR	L24	I	VCLK	Y04	I	THRM# / GPI18	AE03	I	GPI0
B01	**P**	**GND**	E01	IO	AD11	**L25**	**P**	**GND**	Y22	I	PDDRQ	**AE04**	**P**	**VBAT**
B02	**P**	**GND**	E02	IO	AD13	L26	IO	VBE1#	Y23	O	PDA0	AE05	IO	GPIOA / GPIO24
B03	IO	DEVSEL#	E03	IO	AD14	M01	IO	AD27	Y24	O	PDIOR#	AE06	IO	GPIOC / GPIO25
B04	IO	FRAME#	E04	O	GNT2#	M02	IO	AD26	Y25	O	PDIOW#	AE07	IO	LFRM#
B05	IO	AD16	**E05**	**P**	**VCC33**	M03	IO	AD28	Y26	I	PDRDY	AE08	IO	LAD1
B06	IO	AD19	E06	O	GNT0#	M04	O	GNT4#	AA01	IO	EXTSMI# / GPI2	AE09	O	SPKR / strap
B07	IO	GPIO9 / PCREQB	**E07**	**P**	**RAMVCC**	**M22**	**P**	**VCCVK**	AA02	O	SUSA# / GPO1	AE10	I	SERIRQ
B08	IO	GPIO13 / INTF# / PCGNTB	**E08**	**P**	**RAMGND**	**M23**	**P**	**VCCVK**	AA03	OD	GPO0	AE11	IO	SA17 / O17 / strap
B09	IO	MDIO	**E09**	**P**	**GND**	**M24**	**P**	**VCCVK**	**AA04**	**P**	**VSUS33**	AE12	IO	MEMR#
B10	I	MRXCLK	E10	I	MRXD0	**M25**	**P**	**VCCVK**	AA22	IO	PDD15	AE13	IO	XD6
B11	O	MTXD2	**E11**	**P**	**MIIVCC**	**M26**	**P**	**VCCVK**	**AA23**	**P**	**GND**	AE14	IO	XD3
B12	O	MTXENA	**E12**	**P**	**MIIVCC**	N01	IO	AD29	AA24	IO	PDD00	AE15	I	SDDRQ
B13	I	MCRS	**E13**	**P**	**MIIVCC25**	N02	IO	AD31	AA25	IO	PDD01	**AE16**	**P**	**GND**
B14	I	EEDI	E14	I	USBOC5#	N03	IO	AD30	AA26	IO	PDD14	AE17	IO	SDD04 / SA04
B15	I	USBOC1#	E15	I	USBOC3#	N04	I	REQ5# / GPI7	AB01	O	SUSCLK / GPO4	AE18	IO	SDD07 / SA07
B16	**P**	**USBGND**	**E16**	**P**	**GND**	**N22**	**P**	**VCCVK**	AB02	I	SMBALRT#	**AE19**	**P**	**GND**
B17	IO	USBP4–	E17	IO	USBP5+	**N23**	**P**	**VCCVK**	AB03	IO	SMBCK1	AE20	IO	SDD12 / SA12
B18	**P**	**USBGND**	**E18**	**P**	**USBGND**	**N24**	**P**	**VCCVK**	**AB04**	**P**	**VSUS33**	AE21	IO	SDD15 / SA15
B19	IO	USBP2–	E19	IO	USBP3+	**N25**	**P**	**VCCVK**	**AB22**	**P**	**GND**	**AE22**	**P**	**GND**
B20	**P**	**USBGND**	**E20**	**P**	**USBGND**	**N26**	**P**	**VCCVK**	AB23	IO	PDD12	AE23	O	SDA0 / strap
B21	IO	USBP0–	E21	IO	USBP1+	P01	I	INTA#	AB24	IO	PDD02	AE24	I	IRQ14
B22	**P**	**USBGND**	**E22**	**P**	**GNDUPLL**	P02	I	INTB#	**AB25**	**P**	**GND**	**AE25**	**P**	**GND**
B23	**P**	**GNDUPLL**	**E23**	**P**	**GND**	P03	I	INTC#	AB26	IO	PDD13	AE26	IO	PDD06
B24	**P**	**USBVCC**	E24	IO	VAD05	P04	O	GNT5# / GPO7	AC01	I	LID# / GPI4	AF01	O	SUSC#
B25	**P**	**USBVCC**	**E25**	**P**	**GND**	**P22**	**P**	**PLLVCC**	AC02	IO	SMBDT1	AF02	O	SUSB# / GPO2
B26	**P**	**USBVCC**	E26	IO	VAD04	**P23**	**P**	**PLLGND**	AC03	I	GPI1	AF03	O	RTCX2
C01	I	SERR#	F01	IO	AD10	P24	OD	VRDPSLP / GPIO29	**AC04**	**P**	**VSUS33**	AF04	I	PWRGD
C02	IO	PERR#	F02	IO	AD09	P25	OD	VIDSEL / GPIO28	**AC05**	**P**	**VSUS33**	AF05	IO	PCKRUN#
C03	IO	STOP#	F03	IO	AD12	P26	OD	DPSLP# / GPIO23	AC06	IO	GPIOE / 31	AF06	O	PCISTP# / GPO6
C04	IO	IRDY#	F04	IO	CBE0#	R01	I	INTD#	AC07	O	CPUSTP# / GPO5	AF07	IO	LAD3
C05	I	REQ1#	**F22**	**P**	**VCCVK**	R02	O	PCIRST#	**AC08**	**P**	**GND**	AF08	IO	LAD0
C06	IO	AD18	F23	IO	VAD09	R03	O	ACRST#	**AC09**	**P**	**GND**	AF09	I	TEST
C07	IO	GPIO15 / INTH#	F24	IO	VBE0#	**R04**	**P**	**GND**	AC10	IO	IOR#	AF10	IO	MEMW#
C08	I	VGATE / GPIO8 / PCREQA	F25	IO	VAD00	R22	I	PCICLK	AC11	IO	SA19 / O19 / strap	AF11	IO	SA16 / O16 / strap
C09	O	MDCK	F26	IO	VAD01	R23	OD	NMI	AC12	I	OSC	AF12	O	ROMCS#/KBCS#/
C10	I	MRXDV	G01	IO	AD07	R24	OD	GHI# / GPIO22	AC13	IO	XD1	AF13	IO	XD5
C11	O	MTXD3	G02	IO	AD06	R25	OD	INIT#	AC14	IO	XD0	AF14	IO	XD2
C12	O	MTXD0	G03	IO	AD04	R26	OD	STPCLK#	**AC15**	**I**	**SDCOMP**	AF15	IO	SDD00 / SA00
C13	I	MCOL	G04	IO	AD08	T01	O	ACSYNC	**AC16**	**P**	**GND**	AF16	IO	SDD02 / SA02
C14	O	EECK	G22	IO	VAD11	T02	I	ACSDIN0	**AC17**	**P**	**GND**	AF17	IO	SDD03 / SA03
C15	I	USBOC2#	G23	IO	VAD10	T03	I	ACBITCLK	**AC18**	**P**	**VCC33**	AF18	IO	SDD06 / SA06
C16	**P**	**USBGND**	G24	IO	VAD13	**T04**	**P**	**VSUS25**	**AC19**	**P**	**VCC33**	AF19	IO	SDD08 / SA08
C17	**P**	**USBGND**	G25	I	DNSTB	T22	O	APICD0	**AC20**	**P**	**GND**	AF20	IO	SDD11 / SA11
C18	**P**	**USBGND**	G26	I	DNSTB#	T23	OD	INTR	AC21	O	SDIOW#	AF21	IO	SDD14 / SA14
C19	**P**	**USBGND**	H01	IO	AD05	T24	OD	SMI#	AC22	O	SDA1 / strap	AF22	O	SDIOR#
C20	**P**	**USBGND**	H02	IO	AD02	T25	OD	A20M#	AC23	O	SDCS1#	AF23	O	SDA2 / strap
C21	**P**	**USBGND**	H03	IO	AD00	T26	OD	IGNNE#	AC24	IO	PDD04	AF24	I	IRQ15
C22	**P**	**USBGND**	H04	I	REQ3#	U01	O	ACSDOUT	AC25	IO	PDD11	AF25	IO	PDD07
C23	I	USBREXT	H22	IO	VAD12	U02	I	ACSDI2 /IO20/PCS0#	AC26	IO	PDD03	AF26	IO	PDD08
C24	**P**	**USBVCC**	**H23**	**P**	**GND**	U03	I	ACSDIN1	AD01	IO	SMBDT2 / GPIO26			
C25	**P**	**USBVCC**	H24	O	UPSTB	**U04**	**P**	**VSUS25**	AD02	I	PWRBTN#			
C26	**P**	**USBVCC**	**H25**	**P**	**GND**	**U22**	**P**	**VCC**	AD03	I	INTRUD# / GPI16			

GND pins (28 pins): **F6,11, G5, L11-16, M11-16, N5,11-16, P11-16, R11-16, T11-16, V21, W21, AA5, AB5,12-13,18-19**
USBGND pins (4 pins): **F18-21**
VCC pins 18 pins): **F9-10,14-15, H5, J5,21, K5,21, T5,21, U5,21, V5, AB8-9,16-17**
VCC33 pins (25 pins): **F5,7-8,12-13,16-17, L5, M5, P5,21, R5,21, W5, Y5,21, AA21, AB6-7,10-11,14-15,20-21**
VCCVK pins (5 pins): **G21, H21, L21, M21, N21**

Table 2. VT8235 Pin List (Alphabetical Order)

Pin #		Pin Name
T25	OD	A20M#
T03	I	ACBITCLK
R03	O	ACRST#
T02	I	ACSDIN0
U03	I	ACSDIN1
U02	I	ACSDI2 /IO20/PCS0#
V01	I	ACSDI3 /IO21/PCS1# /SLPB#
U01	O	ACSDOUT
T01	O	ACSYNC
H03	IO	AD00
J02	IO	AD01
H02	IO	AD02
J01	IO	AD03
G03	IO	AD04
H01	IO	AD05
G02	IO	AD06
G01	IO	AD07
G04	IO	AD08
F02	IO	AD09
F01	IO	AD10
E01	IO	AD11
F03	IO	AD12
E02	IO	AD13
E03	IO	AD14
D02	IO	AD15
B05	IO	AD16
A05	IO	AD17
C06	IO	AD18
B06	IO	AD19
K01	IO	AD20
J03	IO	AD21
K02	IO	AD22
K03	IO	AD23
L02	IO	AD24
L03	IO	AD25
M02	IO	AD26
M01	IO	AD27
M03	IO	AD28
N01	IO	AD29
N03	IO	AD30
N02	IO	AD31
A08	I	AGPBZ# / GPI6
U23	I	APICCLK
T22	O	APICD0
V23	O	APICD1
W04	I	BATLOW# / GPI5
F04	IO	CBE0#
D01	IO	CBE1#
A04	IO	CBE2#
L01	IO	CBE3#
Y01	I	CPUMISS / GPI17
AC07	O	CPUSTP# / GPO5
B03	IO	DEVSEL#
J24	I	DNCMD
G25	I	DNSTB
G26	I	DNSTB#
P26	OD	DPSLP# / GPIO23
C14	O	EECK
A13	O	EECS#
B14	I	EEDI
A14	O	EEDO
AA01	IO	EXTSMI# / GPI2
U26	I	FERR#
B04	IO	FRAME#
R24	OD	GHI# / GPIO22
A01	**P**	**GND**
A02	**P**	**GND**
B01	**P**	**GND**
B02	**P**	**GND**
E09	**P**	**GND**
E16	**P**	**GND**
E23	**P**	**GND**
E25	**P**	**GND**
H23	**P**	**GND**
H25	**P**	**GND**
K04	**P**	**GND**
L23	**P**	**GND**
L25	**P**	**GND**

Pin #		Pin Name
R04	**P**	**GND**
V04	**P**	**GND**
V22	**P**	**GND**
W25	**P**	**GND**
AA23	**P**	**GND**
AB22	**P**	**GND**
AB25	**P**	**GND**
AC08	**P**	**GND**
AC09	**P**	**GND**
AC16	**P**	**GND**
AC17	**P**	**GND**
AC20	**P**	**GND**
AE16	**P**	**GND**
AE19	**P**	**GND**
AE22	**P**	**GND**
AE25	**P**	**GND**
B23	**P**	**GNDUPLL**
E22	**P**	**GNDUPLL**
E06	O	GNT0#
D05	O	GNT1#
E04	O	GNT2#
J04	O	GNT3#
M04	O	GNT4#
P04	O	GNT5# / GPO7
AE03	I	GPI0
AC03	I	GPI1
B07	IO	GPIO9 / PCREQB
D07	IO	GPIO10
A06	IO	GPIO11
A07	IO	GPIO12/INTE#/PCGA
B08	IO	GPIO13/INTF#/PCGB
D08	IO	GPIO14 / INTG#
C07	IO	GPIO15 / INTH#
AE05	IO	GPIOA / GPIO24
AE06	IO	GPIOC / GPIO25
AD06	IO	GPIOD / 30
AC06	IO	GPIOE / 31
AA03	OD	GPO0
T26	OD	IGNNE#
R25	OD	INIT#
P01	I	INTA#
P02	I	INTB#
P03	I	INTC#
R01	I	INTD#
T23	OD	INTR
AD03	I	INTRUD# / GPI16
AC10	IO	IOR#
AD10	I	IORDY
AD09	IO	IOW#
C04	IO	IRDY#
AE24	I	IRQ14
AF24	I	IRQ15
V03	IO	KBCK / A20G
V02	IO	KBDT / KBRC
AF08	IO	LAD0
AE08	IO	LAD1
AD08	IO	LAD2
AF07	IO	LAD3
AE07	IO	LFRM#
AC01	I	LID# / GPI4
AD07	IO	LREQ#
C13	I	MCOL
B13	I	MCRS
C09	O	MDCK
B09	IO	MDIO
AE12	IO	MEMR#
AF10	IO	MEMW#
D11	**P**	**MIIVCC**
D12	**P**	**MIIVCC**
E11	**P**	**MIIVCC**
E12	**P**	**MIIVCC**
D13	**P**	**MIIVCC25**
E13	**P**	**MIIVCC25**
B10	I	MRXCLK
E10	I	MRXD0
D10	I	MRXD1
D09	I	MRXD2
A09	I	MRXD3

Pin #		Pin Name
C10	I	MRXDV
A10	I	MRXERR
W02	IO	MSCK / IRQ1
W01	IO	MSDT / IRQ12
A12	I	MTXCLK
C12	O	MTXD0
A11	O	MTXD1
B11	O	MTXD2
C11	O	MTXD3
B12	O	MTXENA
R23	OD	NMI
AC12	I	OSC
D03	IO	PAR
AF05	IO	PCKRUN#
R22	I	PCICLK
R02	O	PCIRST#
AF06	O	PCISTP# / GPO6
Y23	O	PDA0
V25	O	PDA1
V26	O	PDA2
W23	**I**	**PDCOMP**
V24	O	PDCS1#
W24	O	PDCS3#
AA24	IO	PDD00
AA25	IO	PDD01
AB24	IO	PDD02
AC26	IO	PDD03
AC24	IO	PDD04
AD25	IO	PDD05
AE26	IO	PDD06
AF25	IO	PDD07
AF26	IO	PDD08
AD24	IO	PDD09
AD26	IO	PDD10
AC25	IO	PDD11
AB23	IO	PDD12
AB26	IO	PDD13
AA26	IO	PDD14
AA22	IO	PDD15
W26	O	PDDACK#
Y22	I	PDDRQ
Y24	O	PDIOR#
Y25	O	PDIOW#
Y26	I	PDRDY
W22	**P**	**PDVREF**
C02	IO	PERR#
P23	**P**	**PLLGND**
P22	**P**	**PLLVCC**
W03	I	PME#
AD02	I	PWRBTN#
AF04	I	PWRGD
AE02	O	PWROK#
E08	**P**	**RAMGND**
E07	**P**	**RAMVCC**
D06	I	REQ0#
C05	I	REQ1#
D04	I	REQ2#
H04	I	REQ3#
L04	I	REQ4#
N04	I	REQ5# / GPI7
Y02	I	RING# / GPI3
AF12	O	ROMCS#/KBCS#/str
AD05	I	RSMRST#
AD04	I	RTCX1
AF03	O	RTCX2
AF11	IO	SA16 / O16 / strap
AE11	IO	SA17 / O17 / strap
AD11	IO	SA18 / O18 / strap
AC11	IO	SA19 / O19 / strap
AE23	O	SDA0 / strap
AC22	O	SDA1 / strap
AF23	O	SDA2 / strap
AC15	**I**	**SDCOMP**
AC23	O	SDCS1#
AD23	O	SDCS3# / strap
AF15	IO	SDD00 / SA00
AD16	IO	SDD01 / SA01
AF16	IO	SDD02 / SA02

Pin #		Pin Name
AF17	IO	SDD03 / SA03
AE17	IO	SDD04 / SA04
AD18	IO	SDD05 / SA05
AF18	IO	SDD06 / SA06
AE18	IO	SDD07 / SA07
AF19	IO	SDD08 / SA08
AD19	IO	SDD09 / SA09
AD20	IO	SDD10 / SA10
AF20	IO	SDD11 / SA11
AE20	IO	SDD12 / SA12
AD21	IO	SDD13 / SA13
AF21	IO	SDD14 / SA14
AE21	IO	SDD15 / SA15
AD22	O	SDDACK#
AE15	I	SDDRQ
AF22	O	SDIOR#
AC21	O	SDIOW#
AD15	I	SDRDY
AD17	**P**	**SDVREF**
AE10	I	SERIRQ
C01	I	SERR#
U25	OD	SLP#
AB02	I	SMBALRT#
AB03	IO	SMBCK1
AE01	IO	SMBCK2 / GPIO27
AC02	IO	SMBDT1
AD01	IO	SMBDT2 / GPIO26
T24	OD	SMI#
AD12	O	SOE# / strap
AE09	O	SPKR / strap
C03	IO	STOP#
R26	OD	STPCLK#
AA02	O	SUSA# / GPO1
AF02	O	SUSB# / GPO2
AF01	O	SUSC#
AB01	O	SUSCLK / GPO4
Y03	O	SUSST1# / GPO3
AF09	I	TEST
Y04	I	THRM# / GPI18
U24	O	TPO
A03	IO	TRDY#
K25	O	UPCMD
H24	O	UPSTB
H26	O	UPSTB#
D23	I	USBCLK
A16	**P**	**USBGND**
A18	**P**	**USBGND**
A20	**P**	**USBGND**
A22	**P**	**USBGND**
B16	**P**	**USBGND**
B18	**P**	**USBGND**
B20	**P**	**USBGND**
B22	**P**	**USBGND**
C16	**P**	**USBGND**
C17	**P**	**USBGND**
C18	**P**	**USBGND**
C19	**P**	**USBGND**
C20	**P**	**USBGND**
C21	**P**	**USBGND**
C22	**P**	**USBGND**
D16	**P**	**USBGND**
D18	**P**	**USBGND**
D20	**P**	**USBGND**
E18	**P**	**USBGND**
E20	**P**	**USBGND**
A15	I	USBOC0#
B15	I	USBOC1#
C15	I	USBOC2#
E15	I	USBOC3#
D14	I	USBOC4#
E14	I	USBOC5#
B21	IO	USBP0–
A21	IO	USBP0+
D21	IO	USBP1–
E21	IO	USBP1+
B19	IO	USBP2–
A19	IO	USBP2+
D19	IO	USBP3–

Pin #		Pin Name
E19	IO	USBP3+
B17	IO	USBP4–
A17	IO	USBP4+
D17	IO	USBP5–
E17	IO	USBP5+
C23	I	USBREXT
A24	**P**	**USBVCC**
A25	**P**	**USBVCC**
A26	**P**	**USBVCC**
B24	**P**	**USBVCC**
B25	**P**	**USBVCC**
B26	**P**	**USBVCC**
C24	**P**	**USBVCC**
C25	**P**	**USBVCC**
C26	**P**	**USBVCC**
D24	**P**	**USBVCC**
F25	IO	VAD00
F26	IO	VAD01
J26	IO	VAD02
J25	IO	VAD03
E26	IO	VAD04
E24	IO	VAD05
K24	IO	VAD06
K26	IO	VAD07
D25	IO	VAD08
F23	IO	VAD09
G23	IO	VAD10
G22	IO	VAD11
H22	IO	VAD12
G24	IO	VAD13
J22	IO	VAD14
K22	IO	VAD15
AE04	**P**	**VBAT**
F24	IO	VBE0#
L26	IO	VBE1#
U22	**P**	**VCC**
E05	**P**	**VCC33**
AC18	**P**	**VCC33**
AC19	**P**	**VCC33**
A23	**P**	**VCCUPLL**
D22	**P**	**VCCUPLL**
F22	**P**	**VCCVK**
L22	**P**	**VCCVK**
M22	**P**	**VCCVK**
M23	**P**	**VCCVK**
M24	**P**	**VCCVK**
M25	**P**	**VCCVK**
M26	**P**	**VCCVK**
N22	**P**	**VCCVK**
N23	**P**	**VCCVK**
N24	**P**	**VCCVK**
N25	**P**	**VCCVK**
N26	**P**	**VCCVK**
L24	I	VCLK
C08	I	VGATE / GPIO8
P25	OD	VIDSEL/GIO28/PCRA
K23	**I**	**VLCOMP**
J23	**P**	**VLVREF**
D26	IO	VPAR
P24	OD	VRDPSLP/GPIO29
T04	**P**	**VSUS25**
U04	**P**	**VSUS25**
AA04	**P**	**VSUS33**
AB04	**P**	**VSUS33**
AC04	**P**	**VSUS33**
AC05	**P**	**VSUS33**
D15	**P**	**VSUSUSB**
AC14	IO	XD0
AC13	IO	XD1
AF14	IO	XD2
AE14	IO	XD3
AD14	IO	XD4
AF13	IO	XD5
AE13	IO	XD6
AD13	IO	XD7

GND pins (28 pins): **F6,11, G5, L11-16, M11-16, N5,11-16, P11-16, R11-16, T11-16, V21, W21, AA5, AB5,12-13,18-19**
USBGND pins (4 pins): **F18-21**
VCC pins 18 pins): **F9-10,14-15, H5, J5,21, K5,21, T5,21, U5,21, V5, AB8-9,16-17**
VCC33 pins (25 pins): **F5,7-8,12-13,16-17, L5, M5, P5,21, R5,21, W5, Y5,21, AA21, AB6-7,10-11,14-15,20-21**
VCCVK pins (5 pins): **G21, H21, L21, M21, N21**

PIN DESCRIPTIONS

Table 3. Pin Descriptions

V-Link Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VAD[15:0]	K22, J22, G24, H22, G22, G23, F23, D25, K26, K24, E24, E26, J25, J26, F26, F25	IO	**Address / Data Bus.** Bits 0-7 are implemented and bits 8-15 are reserved for future use. VAD[6:0] are used to send strap information to the chipset north bridge. At power up VAD[6:4] reflect the state of straps on pins SDA[2:0] and VAD[3:0] reflect the state of straps on pins SA[19:16]. The specific interpretation of these straps is north bridge chip design dependent.
VPAR	D26	IO	**Parity.** If the VPAR function is implemented in a compatible manner on the north bridge, this pin should be connected to the north bridge VPAR pin (P4X333, P4X400, P4X800, KT400). If VPAR is not implemented in the north bridge chip or is incompatible with the 8235 (4x V-Link north bridges) connect this pin to an 8.2K pullup to 2.5V (Pro266, Pro266T, KT266, KT266A, KT333, P4X266, PN266, KN266, KM266, P4M266, P4N266). See app note AN222 for details.
VBE[1:0]#	L26, F24	IO	**Byte Enables.** VBE0# is used with VAD[7-0] and VBE1# is used with VAD[15-8] (VBE1# and VAD[15-8] are reserved for future use).
VCLK	L24	I	**V-Link Clock.**
UPCMD	K25	O	**Command from Client-to-Host.**
DNCMD	J24	I	**Command from Host-to-Client.**
UPSTB	H24	O	**Strobe from Client-to-Host.**
UPSTB#	H26	O	**Complement Strobe from Client-to-Host.**
DNSTB	G25	I	**Strobe from Host-to-Client.**
DNSTB#	G26	I	**Complement Strobe from Host-to-Client.**
VLVREF	J23	I	**Voltage Reference.**
VLCOMP	K23	I	**V-Link Compensation.**
VCCVK	(see pin list)	P	**V-Link VK Power.**

Advanced Programmable Interrupt Controller (APIC) Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
APICD1	V23	O	**Internal APIC Data 1.** Function 0 Rx58[6] = 1
APICD0	T22	O	**Internal APIC Data 0.** Function 0 Rx58[6] = 1
APICCLK	U23	I	**APIC Clock.**

Straps			
Signal Name	**Pin #**	**I/O**	**Signal Description**
Strap / SDCS3#	AD23	I	**Strap.** State reflected on VAD[7] at powerup. No internal function.
Strap / SDA2	AF23	I	**Strap.** State reflected on VAD[6] at powerup. No internal function.
Strap / SDA1	AC22	I	**Strap.** State reflected on VAD[5] at powerup. No internal function.
Strap / SDA0	AE23	I	**Strap.** State reflected on VAD[4] at powerup. No internal function.
Strap / SA19	AC11	I	**Strap.** State reflected on VAD[3] at powerup. No internal function.
Strap / SA18	AD11	I	**Strap.** State reflected on VAD[2] at powerup. No internal function.
Strap / SA17	AE11	I	**Strap.** State reflected on VAD[1] at powerup. No internal function.
Strap / SA16	AF11	I	**Strap.** State reflected on VAD[0] at powerup. No internal function.
Strap / SOE#	AD12	I	**Strap.** Strap low to enable (high to disable) auto reboot.
Strap / SPKR	AE9	I	**Strap.** Strap low to enable (high to disable) CPU frequency strapping
Strap / ROMCS# / KBCS#	AF12	I	**Strap.** Strap high to enable LPC BIOS ROM

CPU Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
A20M#	T25	OD	**A20 Mask.** Connect to A20 mask input of the CPU to control address bit-20 generation. Logical combination of the A20GATE input (from internal or external keyboard controller) and Port 92 bit-1 (Fast_A20).
FERR#	U26	I	**Numerical Coprocessor Error.** This signal is tied to the coprocessor error signal on the CPU. Internally generates interrupt 13 if active. Output voltage swing is programmable tot 1.5V or 2.5V by Device 17 Function 0 Rx67[2].
IGNNE#	T26	OD	**Ignore Numeric Error.** This pin is connected to the CPU "ignore error" pin.
INIT#	R25	OD	**Initialization.** The VT8235 asserts INIT# if it detects a shut-down special cycle on the PCI bus or if a soft reset is initiated by the register
INTR	T23	OD	**CPU Interrupt.** INTR is driven by the VT8235 to signal the CPU that an interrupt request is pending and needs service.
NMI	R23	OD	**Non-Maskable Interrupt.** NMI is used to force a non-maskable interrupt to the CPU. The VT8235 generates an NMI when PCI bus SERR# is asserted.
SLP#	U25	OD	**Sleep.** Used to put the CPU to sleep.
SMI#	T24	OD	**System Management Interrupt.** SMI# is asserted by the VT8235 to the CPU in response to different Power-Management events.
STPCLK#	R26	OD	**Stop Clock.** STPCLK# is asserted by the VT8235 to the CPU to throttle the processor clock.

Note: Connect each of the above signals to 150 Ω pullup resistors to VCC_CMOS (see Design Guide).

CPU Speed Control Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VGATE / GPIO8 / PCREQA	C8	I	**Voltage Gate.** Signal from the CPU voltage regulator. High indicates the voltage regulator output is stable. This pin performs the VGATE function if Device 17 Function 0 Rx53[7] = 0, E5[4] = 1 and E4[3] = 0.
VIDSEL / GPIO28	P25	OD	**Voltage Regulator ID Select.** Connected to the CPU voltage regulator. Low selects the voltage ID from the CPU; high selects a different fixed voltage ID (the lower voltage used for CPU deep sleep mode). This pin performs the VIDSEL function if Func 0 RxE5[3] = 0.
VRDSLP / GPIO29	P24	OD	**Voltage Regulator Deep Sleep.** Connected to the CPU voltage regulator. High selects the proper voltage for deep sleep mode. This pin performs the VRDPSLP function if Function 0 RxE5[3] = 0.
GHI# / GPIO22	R24	OD	**CPU Speed Select.** Connected to the CPU voltage regulator, used to select high speed (L) or low speed (H). This pin performs the GHI# function if Function 0 RxE5[3] = 0.
DPSLP# / GPIO23	P26	OD	**CPU Deep Sleep.**
CPUMISS / GPI17	Y1	I	**CPU Missing.** Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to the CPUMISS pin of the CPU socket. The state of this pin may be read in the SMBus 2 registers. This pin may be used as CPUMISS and GPI17 at the same time.
AGPBZ# / GPI6	A8	I	**AGP Busy.** Low indicates that an AGP master cycle is in progress (CPU speed transitions will be postponed if this input is asserted low). Connected to the AGP Bus AGPBZ# pin.

Summary of Internal Pull-Up / Pull-Down Resistor Implementation

Internal Pullups are present on pins KBCK, KBDT, MSCK, MSDT, SERIRQ, LAD[3:0]

Internal Pulldowns are present on pins SA[19-16] and all LAN pins

PCI Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
AD[31:0]	(see pin list)	IO	**Address / Data Bus.** Multiplexed address and data. The address is driven with FRAME# assertion and data is driven or received in following cycles.
CBE[3:0]#	L1, A4, D1, F4	IO	**Command / Byte Enable.** The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
DEVSEL#	B3	IO	**Device Select.** The VT8235 asserts this signal to claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VT8235-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle.
FRAME#	B4	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
IRDY#	C4	IO	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
TRDY#	A3	IO	**Target Ready.** Asserted when the target is ready for data transfer.
STOP#	C3	IO	**Stop.** Asserted by the target to request the master to stop the current transaction.
SERR#	C1	I	**System Error.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the VT8235 can be programmed to generate an NMI to the CPU.
PAR	D3	IO	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]#.
INTA# **INTB#** **INTC#** **INTD#** **INTE#** / GPIO12 / PCGNTA, **INTF#** / GPIO13 / PCGNTB, **INTG#** / GPIO14, **INTH#** / GPIO15	P1, P2, P3, R1 A7, B8, D8, C7	I	**PCI Interrupt Request**. The INTA# through INTD# pins are typically connected to the PCI bus INTA#-INTD# pins per the table below. INTE-H# are enabled by setting Device 17, Function 0 Rx5B[1] = 1. BIOS settings must match the physical connection method. — INTA# / INTB# / INTC# / INTD# PCI Slot 1 — INTA# / INTB# / INTC# / INTD# PCI Slot 2 — INTB# / INTC# / INTD# / INTE# PCI Slot 3 — INTC# / INTD# / INTE# / INTF# PCI Slot 4 — INTD# / INTE# / INTF# / INTG# PCI Slot 5 — INTE# / INTF# / INTG# / INTH# PCI Slot 6 — INTF# / INTG# / INTH# / INTA#
REQ5# / GPI7, **REQ4#,** **REQ3#,** **REQ2#,** **REQ1#,** **REQ0#**	N4 L4 H4 D4 C5 D6	I	**PCI Request.** These signals connect to the VT8235 from each PCI slot (or each PCI master) to request the PCI bus. To use pin N4 as REQ5#, Function 0 RxE4 must be set to 1 otherwise this pin will function as General Purpose Input 7.
GNT5# / GPO7, **GNT4#,** **GNT3#,** **GNT2#,** **GNT1#,** **GNT0#**	P4 M4 J4 E4 D5 E6	O	**PCI Grant.** These signals are driven by the VT8235 to grant PCI access to a specific PCI master. To use pin P4 as GNT5#, Function 0 RxE4 must be set to 1 otherwise this pin will function as General Purpose Output 7.
PCIRST#	R2	O	**PCI Reset.** This signal is used to reset devices attached to the PCI bus.
PCICLK	R22	I	**PCI Clock.** This signal provides timing for all transactions on the PCI Bus.
PCKRUN#	AF5	IO	**PCI Bus Clock Run.** This signal indicates whether the PCI clock is or will be stopped (high) or running (low). The VT8235 drives this signal low when the PCI clock is running (default on reset) and releases it when it stops the PCI clock. External devices may assert this signal low to request that the PCI clock be restarted or prevent it from stopping. Connect this pin to ground using a 100 Ω resistor if the function is not used. Refer to the "PCI Mobile Design Guide" and the VIA "VT8633 Apollo Pro266 Design Guide" for more details.

LAN Controller - Media Independent Interface (MII)				
Signal Name	**Pin #**	**I/O**	**PU**	**Signal Description**
MCOL	C13	I	***PD***	**MII Collision Detect.** From the external PHY.
MCRS	B13	I	***PD***	**MII Carrier Sense.** Asserted by the external PHY when the media is active.
MDCK	C9	O	***PD***	**MII Management Data Clock.** Sent to the external PHY as a timing reference for MDIO
MDIO	B9	IO	***PD***	**MII Management Data I/O.** Read from the MDI bit or written to the MDO bit.
MRXCLK	B10	I	***PD***	**MII Receive Clock.** 2.5 or 25 MHz clock recovered by the PHY.
MRXD[3-0]	A9, D9, D10, E10	I	***PD***	**MII Receive Data.** Parallel receive data lines driven by the external PHY synchronous with MRXCLK.
MRXDV	C10	I	***PD***	**MII Receive Data Valid.**
MRXERR	A10	I	***PD***	**MII Receive Error.** Asserted by the PHY when it detects a data decoding error.
MTXCLK	A12	I	***PD***	**MII Transmit Clock.** Always active 2.5 or 25 MHz clock supplied by the PHY.
MTXD[3-0]	C11, B11, A11, C12	O	***PD***	**MII Transmit Data.** Parallel transmit data lines synchronized to MTXCLK.
MTXENA	B12	O	***PD***	**MII Transmit Enable.** Signals that transmit is active from the MII port to the PHY.
MIIVCC	D11, D12, E11, E12	**Power**		**MII Interface Power.** 3.3V ±5%.
MIIVCC25	D13, E13	**Power**		**MII Suspend Power.** 2.5V ±5%.
RAMVCC	E7	**Power**		**Power For Internal LAN RAM.** 2.5V ±5%.
RAMGND	E8	**Power**		**Ground For Internal LAN RAM.**

Serial EEPROM Interface				
Signal Name	**Pin #**	**I/O**	**PU**	**Signal Description**
EECS#	A13	O		**Serial EEPROM Chip Select.**
EECK	C14	O		**Serial EEPROM Clock.**
EEDO	A14	O		**Serial EEPROM Data Output.**
EEDI	B14	I		**Serial EEPROM Data Input.**

These pins are disabled if the SDCS1# pin is strapped low to enable serial EEPROM connection via the MII interface.

Low Pin Count (LPC) Interface				
Signal Name	**Pin #**	**I/O**	**PU**	**Signal Description**
LFRM#	AE7	IO		**LPC Frame.**
LREQ#	AD7	IO		**LPC DMA / Bus Master Request.**
LAD[3-0]	AF7, AD8, AE8, AF8	IO	PU	**LPC Address / Data.**

Note: Connect the LPC interface LPCRST# (LPC Reset) signal to PCIRST#

PC / PCI DMA				
Signal Name	**Pin #**	**I/O**	**PU**	**Signal Description**
PCREQA / GPIO8 / VGATE	C8	I		**PC / PCI Request A.** Device 17 Function 0 Rx53[7] = 1
PCREQB / GPIO9	B7	I		**PC / PCI Request B.** Device 17 Function 0 Rx53[7] = 1
PCGNTA / GPIO12	A7	O		**PC / PCI Grant A.** Device 17 Function 0 Rx53[7] = 1
PCGNTB / GPIO13	B8	O		**PC / PCI Grant B.** Device 17 Function 0 Rx53[7] = 1

Universal Serial Bus 2.0 Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
USBP0+	A21	IO	**USB 2.0 Port 0 Data +**
USBP0–	B21	IO	**USB 2.0 Port 0 Data –**
USBP1+	E21	IO	**USB 2.0 Port 1 Data +**
USBP1–	D21	IO	**USB 2.0 Port 1 Data –**
USBP2+	A19	IO	**USB 2.0 Port 2 Data +**
USBP2–	B19	IO	**USB 2.0 Port 2 Data –**
USBP3+	E19	IO	**USB 2.0 Port 3 Data +**
USBP3–	D19	IO	**USB 2.0 Port 3 Data –**
USBP4+	A17	IO	**USB 2.0 Port 4 Data +**
USBP4–	B17	IO	**USB 2.0 Port 4 Data –**
USBP5+	E17	IO	**USB 2.0 Port 5 Data +**
USBP5–	D17	IO	**USB 2.0 Port 5 Data –**
USBCLK	D23	I	**USB 2.0 Clock.** 48MHz clock input for the USB interface
USBOC0#	A15	I	**USB 2.0 Port 0 Over Current Detect.** Port 0 is disabled if low.
USBOC1#	B15	I	**USB 2.0 Port 1 Over Current Detect.** Port 1 is disabled if low.
USBOC2#	C15	I	**USB 2.0 Port 2 Over Current Detect.** Port 2 is disabled if low.
USBOC3#	E15	I	**USB 2.0 Port 3 Over Current Detect.** Port 3 is disabled if low.
USBOC4#	D14	I	**USB 2.0 Port 4 Over Current Detect.** Port 4 is disabled if low.
USBOC5#	E14	I	**USB 2.0 Port 5 Over Current Detect.** Port 5 is disabled if low.
USBVCC	(see pin list)	**Power**	**USB 2.0 Port Differential Output Interface Logic Voltage.** 3.3V
USBGND	(see pin list)	**Power**	**USB 2.0 Port Differential Output Interface Logic Ground.**
VSUSUSB	D15	**Power**	**USB 2.0 Suspend Power.** 2.5V ±5%.
VCCUPLL	A23, D22	**Power**	**USB 2.0 PLL Analog Voltage.** 2.5V ±5%.
GNDUPLL	B23, E22	**Power**	**USB 2.0 PLL Analog Ground.**

System Management Bus (SMB) Interface (I^2C Bus)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
SMBCK1	AB3	IO	**SMB / I^2C Channel 1 Clock.**
SMBCK2 / GPI27 / GPO27	AE1	IO	**SMB / I^2C Channel 2 Clock.** Rx95[2] = 0
SMBDT1	AC2	IO	**SMB / I^2C Channel 1 Data.**
SMBDT2 / GPI26 / GPO26	AD1	IO	**SMB / I^2C Channel 2 Data.** Rx95[2] = 0
SMBALRT#	AB2	I	**SMB Alert.** (enabled by System Management Bus I/O space Rx08[3] = 1) When the chip is enabled to allow it, assertion generates an IRQ or SMI interrupt or a power management resume event. Connect to a 10K ohm pullup to VSUS33 if not used.

Programmable Chip Selects			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PCS0# / GPIO20 / ACSDIN2	U2	O	**Programmable Chip Select 0.** RxE4[6]=1, E5[1]=1
PCS1# / GPIO21 / ACSDIN3 / SLPBTN#	V1	O	**Programmable Chip Select 1.** RxE4[6]=1, E5[2]=1

UltraDMA-133 / 100 / 66 / 33 Enhanced IDE Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PDRDY / PDDMARDY / PDSTROBE	Y26	I	EIDE Mode: **Primary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Primary Device DMA Ready**. Output flow control. The device may assert DDMARDY to pause output transfers **Primary Device Strobe**. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
SDRDY / SDDMARDY / SDSTROBE	AD15	I	EIDE Mode: **Secondary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Secondary Device DMA Ready**. Output flow control. The device may assert DDMARDY to pause output transfers **Secondary Device Strobe**. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
PDIOR# / PHDMARDY / PHSTROBE	Y24	O	EIDE Mode: **Primary Device I/O Read.** Device read strobe UltraDMA Mode: **Primary Host DMA Ready**. Primary channel input flow control**.** The host may assert HDMARDY to pause input transfers **Primary Host Strobe**. Output data strobe (both edges). The host may stop HSTROBE to pause output data transfers
SDIOR# / SHDMARDY / SHSTROBE	AF22	O	EIDE Mode: **Secondary Device I/O Read.** Device read strobe UltraDMA Mode: **Secondary Host DMA Ready**. Input flow control. The host may assert HDMARDY to pause input transfers **Host Strobe B**. Output strobe (both edges). The host may stop HSTROBE to pause output data transfers
PDIOW# / PSTOP	Y25	O	EIDE Mode: **Primary Device I/O Write.** Device write strobe UltraDMA Mode: **Primary Stop**. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
SDIOW# / SSTOP	AC21	O	EIDE Mode: **Secondary Device I/O Write.** Device write strobe UltraDMA Mode: **Secondary Stop**. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
PDDRQ	Y22	I	**Primary Device DMA Request.** Primary channel DMA request
SDDRQ	AE15	I	**Secondary Device DMA Request.** Secondary channel DMA request
PDDACK#	W26	O	**Primary Device DMA Acknowledge.** Primary channel DMA acknowledge
SDDACK#	AD22	O	**Secondary Device DMA Acknowledge.** Secondary channel DMA acknowledge
IRQ14	AE24	I	**Primary Channel Interrupt Request.**
IRQ15	AF24	I	**Secondary Channel Interrupt Request.**

UltraDMA-133 / 100 / 66 / 33 Enhanced IDE Interface (continued)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PDCS1#	V24	O	**Primary Master Chip Select.** This signal corresponds to CS1FX# on the primary IDE connector.
PDCS3#	W24	O	**Primary Slave Chip Select.** This signal corresponds to CS3FX# on the primary IDE connector.
SDCS1# / strap	AC23	O	**Secondary Master Chip Select.** This signal corresponds to CS17X# on the secondary IDE connector. Strap low (resistor to ground) to enable serial EEPROM interface via the MII bus (this disables the EExx pins). This pin has an internal pullup to default to serial EEPROM interface via the Eexx pins.
SDCS3# / strap	AD23	O	**Secondary Slave Chip Select.** This signal corresponds to CS37X# on the secondary IDE connector. Strap information is communicated to the north bridge via VAD[7].
PDA[2-0]	V26, V25, Y23	O	**Primary Disk Address.** PDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
SDA[2-0] / strap	AF23, AC22, AE23	O	**Secondary Disk Address.** SDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed. Strap information is communicated to the north bridge via VAD[6:4].
PDD[15-0]	(see pin list)	IO	**Primary Disk Data.**
SDD[15-0] / SA[15-0]	(see pin list)	IO / IO	**Secondary Disk Data.**
PDCOMP	W23	I	**Primary Disk Compensation.**
SDCOMP	AC15	I	**Secondary Disk Compensation.**

Serial IRQ			
Signal Name	**Pin #**	**I/O**	**Signal Description**
SERIRQ	AE10	I	**Serial IRQ.** This pin has an internal pull-up resistor.

AC97 Audio / Modem Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
ACRST#	R3	O	**AC97 Reset.**
ACBTCK	T3	I	**AC97 Bit Clock.**
ACSYNC	T1	O	**AC97 Sync.**
ACSDO	U1	O	**AC97 Serial Data Out.**
ACSDIN0 (VSUS33)†	T2	I	**AC97 Serial Data In 0.**
ACSDIN1 (VSUS33)†	U3	I	**AC97 Serial Data In 1.**
ACSDIN2 / GPIO20 / PCS0#	U2	I	**AC97 Serial Data In 2.** RxE4[6]=0,E5[1]=0, PMIO Rx4C[20]=1
ACSDIN3 / GPIO21 / PCS1# / SLPBTN#	V1	I	**AC97 Serial Data In 3.** RxE4[6]=0,E5[2]=0, PMIO Rx4C[21]=1

†The supply voltage for ACSDIN0-1 is VSUS33 so these inputs can support wake-up on modem ring.

Internal Keyboard Controller

Signal Name	Pin #	I/O	PU	Signal Description
MSCK / IRQ1	W2	IO / I	PU	**MultiFunction Pin** (Internal mouse controller enabled by Rx51[1]) Rx51[2]=1 **Mouse Clock.** From internal mouse controller. Rx51[2]=0 **Interrupt Request 1**. Interrupt input 1.
MSDT / IRQ12	W1	IO / I	PU	**MultiFunction Pin** (Internal mouse controller enabled by Rx51[1]) Rx51[2]=1 **Mouse Data.** From internal mouse controller. Rx51[2]=0 **Interrupt Request 12**. Interrupt input 12.
KBCK / KA20G	V3	IO / I	PU	**MultiFunction Pin** (Internal keyboard controller enabled by Rx51[0]) Rx51[0]=1 **Keyboard Clock.** From internal keyboard controller Rx51[0]=0 **Gate A20.** Input from external keyboard controller.
KBDT / KBRC	V2	IO / I	PU	**MultiFunction Pin** (Internal keyboard controller enabled by Rx51[0]) Rx51[0]=1 **Keyboard Data.** From internal keyboard controller. Rx51[0]=0 **Keyboard Reset.** From external keyboard controller (KBC) for CPURST# generation
KBCS# / ROMCS# / strap	AF12	O / O		**Keyboard Chip Select** (Rx51[0]=0). To external keyboard controller chip. Strap high to enable LPC ROM:

Note: KBCK, KBDT, MSCK, and MSDT are powered by the VSUS33 suspend voltage plane.

ISA Subset / Parallel BIOS ROM Interface

Signal Name	Pin #	I/O	PU	Signal Description
ROMCS# / KBCS# / strap	AF12	O		**ROM Chip Select** (Rx51[0]=1). Chip Select to the BIOS ROM. Strap high to enable LPC ROM.
SPKR / strap	AE9	O		**Speaker.** Strap low to enable (high to disable) CPU frequency strapping.
MEMR#	AE12	O		**Memory Read.**
MEMW#	AF10	O		**Memory Write.**
IOR#	AC10	O		**I/O Read.**
IOW#	AD9	O		**I/O Write.**
IORDY / GPI19	AD10	I		**I/O Ready.** Used to insert wait states in I/O or memory cycles. RxE5[0] = 0
SOE# / strap	AD12	O		**XD Bus Tranceiver Output Enable.** Strap low to enable auto reboot.
XD[7-0]	AD13, AE13, AF13, AD14, AE14, AF14, AC13, AC14	IO		**XD Bus.** For input of BIOS ROM data or data from other on-board I/O or memory devices.
SA[19-16] / GPO[19-16] / straps	AC11, AD11, AE11, AF11	O	***PD***	**System Address 19-16.** Strap states are passed to North Bridge via VAD[3-0]. Functions as SA[19-16] if RxE4[5] = 0.
SA[15-0] / SDD[15-0]	(see pin list)	O		**System Address 15-0.**

General Purpose Inputs				
Signal Name		**Pin #**	**I/O**	**Signal Description**
<u>**GPI0**</u>	***(VBAT)***	AE3	I	**General Purpose Input 0.** Status on PMIO Rx20[0]
<u>**GPI1**</u>	***(VSUS33)***	AC3	I	**General Purpose Input 1.** Status on PMIO Rx20[1]
<u>**GPI2**</u> / EXTSMI#	***(VSUS33)***	AA1	I	**General Purpose Input 2.** Status on PMIO Rx20[4]
<u>**GPI3**</u> / RING#	***(VSUS33)***	Y2	I	**General Purpose Input 3.** Status on PMIO Rx20[8]
<u>**GPI4**</u> / LID#	***(VSUS33)***	AC1	I	**General Purpose Input 4.** Status on PMIO Rx20[11]
<u>**GPI5**</u> / BATLOW#	***(VSUS33)***	W4	I	**General Purpose Input 5.** Status on PMIO Rx20[12]
<u>**GPI6**</u> / AGPBZ#		A8	I	**General Purpose Input 6.** Status on PMIO Rx20[5]
<u>**GPI7**</u> / REQ5#		N4	I	**General Purpose Input 7.** RxE4[2] = 0
<u>**GPI8**</u> / GPO8 / PCREQA / VGATE		C8	I	**General Purpose Input 8.** RxE4[3] = 0, E5[4]=0, 53[7] = 0
<u>**GPI9**</u> / GPO9 / PCREQB		B7	I	**General Purpose Input 9.** RxE4[3] = 0, 53[7] = 0
<u>**GPI10**</u> / GPO10		D7	I	**General Purpose Input 10.** RxE4[3] = 0
<u>**GPI11**</u> / GPO11		A6	I	**General Purpose Input 11.** RxE4[3] = 0
<u>**GPI12**</u> / GPO12 / INTE# / PCGNTA		A7	I	**General Purpose Input 12.** RxE4[4] = 0, 5B[1]=0, 53[7]=0
<u>**GPI13**</u> / GPO13 / INTF# / PCGNTB		B8	I	**General Purpose Input 13.** RxE4[4] = 0, 5B[1]=0, 53[7]=0
<u>**GPI14**</u> / GPO14 / INTG#		D8	I	**General Purpose Input 14.** RxE4[4] = 0, 5B[1]=0
<u>**GPI15**</u> / GPO15 / INTH#		C7	I	**General Purpose Input 15.** RxE4[4] = 0, 5B[1]=0
<u>**GPI16**</u> / <u>INTRUDER#</u>	***(VBAT)***	AD3	I	**General Purpose Input 16.** Status on PMIO Rx20[6]
<u>**GPI17**</u> / <u>CPUMISS</u>		Y1	I	**General Purpose Input 17.** Status on PMIO Rx20[5]
<u>**GPI18**</u> / <u>THRM#</u> / AOLGPI		Y4	I	**General Purpose Input 18.** Rx8C[3] = 0
GPI19 / <u>IORDY</u>		AD10	I	**General Purpose Input 19.** RxE5[0] = 1
<u>**GPI20**</u> / GPO20 / <u>ACSDIN2</u> / PCS0#		U2	I	**General Purpose Input 20.** RxE4[6]=1, E5[1]=0, PMIO 4C[20] = 1
<u>**GPI21**</u> / GPO21 / <u>ACSDIN3</u> / PCS1# / SLPBTN#		V1	I	**General Purpose Input 21.** RxE4[6]=1, E5[2]=0 PMIO 4C[21] = 1
<u>**GPI22**</u> / GPO22 / GHI#		R24	I	**General Purpose Input 22.** RxE5[3] = 1, PMIO 4C[22] = 1
<u>**GPI23**</u> / GPO23 / DPSLP#		P26	I	**General Purpose Input 23.** RxE5[3] = 1, PMIO 4C[23] = 1
<u>**GPI24**</u> / GPO24 / GPIOA		AE5	I	**General Purpose Input 24.** RxE6[0] = 0
<u>**GPI25**</u> / GPO25 / GPIOC		AE6	I	**General Purpose Input 25.** RxE6[1] = 0
GPI26 / GPO26 / <u>SMBDT2</u>	***(VSUS33)***	AD1	I	**General Purpose Input 26.** Rx95[2] = 1, 95[3] = 0
GPI27 / GPO27 / <u>SMBCK2</u>	***(VSUS33)***	AE1	I	**General Purpose Input 27.** Rx95[2] = 1, 95[3] = 0
<u>**GPI28**</u> / GPO28 / VIDSEL		P25	I	**General Purpose Input 28.** RxE5[3] = 1, PMIO 4C[28] = 1
<u>**GPI29**</u> / GPO29 / VRDSLP		P24	I	**General Purpose Input 29.** RxE5[3] = 1, PMIO 4C[29] = 1
<u>**GPI30**</u> / GPO30 / GPIOD		AD6	I	**General Purpose Input 30.** RxE6[6] = 0
<u>**GPI31**</u> / GPO31 / GPIOE		AC6	I	**General Purpose Input 31.** RxE6[7] = 0

Note: Default pin function is underlined in the signal name column above.
Note: Input pin status for the above GPI pins 31-0 is also available on PMIO Rx4B-48[31-0]
Note: See also Power Management I/O register Rx50 for input pin change status for GPI16-19 and 24-27
Note: See also Power Management I/O register Rx52 for SCI/SMI select for GPI16-19 and 24-27
Note: See also Power Management I/O register Rx4C. General purpose input pins 20-31 are shared with OD (open drain) general purpose output functions, so to use one of these pins as an input pin, a one must be written to the corresponding bit of PMIO Rx4C.

General Purpose I/O			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GPIOA / GPI24 / GPO24	AE5	IO	**General Purpose I/O A / 24.** RxE6[0] = 1
GPIOC / GPI25 / GPO25	AE6	IO	**General Purpose I/O C / 25.**
GPIOD / GPI30 / GPO30	AD6	IO	**General Purpose I/O D / 30.**
GPIOE / GPI31 / GPO31	AC6	IO	**General Purpose I/O E / 31.**

The output type of the above pins may be selected as either OD or TTL (see Device 17 Function 0 RxE7)

General Purpose Outputs			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GPO0 ***(VSUS33)***	AA3	OD	**General Purpose Output 0.**
GPO1 / SUSA# ***(VSUS33)***	AA2	O	**General Purpose Output 1.** Rx94[2] = 1
GPO2 / SUSB# ***(VSUS33)***	AF2	O	**General Purpose Output 2.** Rx94[3] = 1
GPO3 / SUSST1# ***(VSUS33)***	Y3	O	**General Purpose Output 3.** Rx94[4] = 1
GPO4 / SUSCLK ***(VSUS33)***	AB1	O	**General Purpose Output 4.** Rx95[1] = 1
GPO5 / CPUSTP#	AC7	O	**General Purpose Output 5.** RxE4[0] = 1
GPO6 / PCISTP#	AF6	O	**General Purpose Output 6.** RxE4[1] = 1
GPO7 /GNT5#	P4	O	**General Purpose Output 7.** RxE4[2] = 0
GPO8 / GPI8 / PCREQA / VGATE	C8	O	**General Purpose Output 8.** RxE4[3]=1, E5[4]=0, 53[7]=0
GPO9 / GPI9 / PCREQB	B7	O	**General Purpose Output 9.** RxE4[3]=1, 53[7]=0
GPO10 / GPI10	D7	O	**General Purpose Output 10.** RxE4[3]=1
GPO11 / GPI11	A6	O	**General Purpose Output 11.** RxE4[3]=1
GPO12 / GPI12 / INTE# / PCGNTA	A7	O	**General Purpose Output 12.** RxE4[4]=1, 5B[1]=0, 53[7]=0
GPO13 / GPI13 / INTF# / PCGNTB	B8	O	**General Purpose Output 13.** RxE4[4]=1, 5B[1]=0, 53[7]=0
GPO14 / GPI14 / INTG#	D8	O	**General Purpose Output 14.** RxE4[4]=1, 5B[1]=0
GPO15 / GPI15 / INTH#	C7	O	**General Purpose Output 15.** RxE4[4]=1, 5B[1]=0
GPO16 / SA16 / strap	AF11	O	**General Purpose Output 16.** RxE4[5] = 1
GPO17 / SA17 / strap	AE11	O	**General Purpose Output 17.** RxE4[5] = 1
GPO18 / SA18 / strap	AD11	O	**General Purpose Output 18.** RxE4[5] = 1
GPO19 / SA19 / strap	AC11	O	**General Purpose Output 19.** RxE4[5] = 1
GPO20 / GPI20 / ACSDIN2 / PCS0#	U2	OD	**General Purpose Output 20.** RxE4[6]=1, E5[1]=0
GPO21 / GPI21 / ACSDIN3 / PCS1# /SLPBTN#	V1	OD	**General Purpose Output 21.** RxE4[6]=1, E5[2]=0
GPO22 / GPI22 / GHI#	R24	OD	**General Purpose Output 22.** RxE5[3]=1, PMIO 4C[22]=1
GPO23 / GPI23 / DPSLP#	P26	OD	**General Purpose Output 23.** RxE5[3]=1, PMIO 4C[23]=1
GPO24 / GPI24 / GPIOA	AE5	O/OD	**General Purpose Output 24.** RxE6[0] = 1
GPO25 / GPI25 / GPIOC	AE6	O/OD	**General Purpose Output 25.** RxE6[1] = 1
GPO26 / GPI26 / SMBDT2 ***(VSUS33†)***	AD1	OD	**General Purpose Output 26.** Rx95[2] = 1, 95[3] = 1
GPO27 / GPI27 / SMBCK2 ***(VSUS33†)***	AE1	OD	**General Purpose Output 27.** Rx95[2] = 1, 95[3] = 1
GPO28 / GPI28 / VIDSEL	P25	OD	**General Purpose Output 28.** RxE5[3] = 1, PMIO 4C[28]=1
GPO29 / GPI29 / VRDSLP	P24	OD	**General Purpose Output 29.** RxE5[3] = 1, PMIO 4C[29]=1
GPO30 / GPI30 / GPIOD	AD6	O/OD	**General Purpose Output 30.** RxE6[6] = 1
GPO31 / GPI31 / GPIOE	AC6	O/OD	**General Purpose Output 31.** RxE6[7] = 1

Note: The output state for each of the above general purpose outputs is selectable via Power Management I/O registers Rx4C-48
Note: The output types of GPO24-25 and 30-31 are selectable OD vs TTL (see Function 0 RxE7)
Note: Default pin functions are underlined in the table above.
† The suspend voltage is only used for maintaining the operation of the SMB function on thses pins (Device 17 Function 0 Rx95[3] = 0). If VCC power is lost, the GPIO function of these pins and the state of PMIO Rx4C[27:26} (which determines the GPO output level) will be lost also.

Power Management and Event Detection

Signal Name	Pin #	I/O	Signal Description
PWRBTN#	AD2	I	**Power Button.** Used by the Power Management subsystem to monitor an external system on/off button or switch. Internal logic powered by VSUS33.
SLPBTN# / GPIO21 / ACSDIN3 / PCS1#	V1	I	**Sleep Button.** Used by the Power Management subsystem to monitor an external sleep button or switch. RxE4[6] = 1, 80[6] = 1, E5[2] = 0 and PMIO Rx4C[21] = 1
RSMRST#	AD5	I	**Resume Reset.** Resets the internal logic connected to the VSUS33 power plane and also resets portions of the internal RTC logic. Internal logic powered by VBAT.
EXTSMI# / GPI2	AA1	IOD	**External System Management Interrupt.** When enabled to allow it, a falling edge on this input causes an SMI# to be generated to the CPU to enter SMI mode. (10K PU to VSUS33 if not used) (3.3V only)
PME#	W3	I	**Power Management Event.** (10K PU to VSUS33 if not used)
SMBALRT#	AB2	I	**SMB Alert**. When programmed to allow it (SMB I/O Rx8[3]=1), assertion generates an IRQ, SMI, or power management event. (10K PU to VSUS33 if not used)
LID# / GPI4	AC1	I	**Notebook Computer Display Lid Open / Closed Monitor.** Used by the Power Management subsystem to monitor the opening and closing of the display lid of notebook computers. Can be used to detect either low-to-high or high-to-low transitions to generate an SMI#. (10K PU to VSUS33 if not used)
INTRUDER# / GPI16	AD3	I	**Intrusion Indicator.** The value of this bit may be read at PMIO Rx20[6]
THRM# / GPI18 / AOLGPI	Y4	I	**Thermal Alarm Monitor.** Rx8C[3] = 1. Rising or falling edges (selectable by PMIO Rx2C[6]) may be detected to set status at PMIO Rx20[10]. Setting of this status bit may then be used to generate an SCI or SMI. THRM# may also be used to enable duty cycle control of stop-clock (STPCLK#) to automatically limit maximum temperature (see Device 17 Function 0 Rx8C[7-3]).
RING# / GPI3	Y2	I	**Ring Indicator.** May be connected to external modem circuitry to allow the system to be re-activated by a received phone call. (10K PU to VSUS33 if not used)
BATLOW# / GPI5	W4	I	**Battery Low Indicator.** (10K PU to VSUS33 if not used) (3.3V only)
CPUSTP# / GPO5	AC7	O	**CPU Clock Stop** (RxE4[0] = 0). Signals the system clock generator to disable the CPU clock outputs. Not connected if not used.
PCISTP# / GPO6	AF6	O	**PCI Clock Stop** (RxE4[1] = 0). Signals the system clock generator to disable the PCI clock outputs. Not connected if not used.
SUSA# / GPO1	AA2	O	**Suspend Plane A Control** (Rx94[2]=0). Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane. (10K PU to VSUS33 if not used)
SUSB# / GPO2	AF2	O	**Suspend Plane B Control** (Rx94[3]=0). Asserted during power management STR and STD suspend states. Used to control the secondary power plane. (10K PU to VSUS33 if not used)
SUSC#	AF1	O	**Suspend Plane C Control.** Asserted during power management STD suspend state. Used to control the tertiary power plane. Also connected to ATX power-on circuitry. (10K PU to VSUS33 if not used)
SUSST1# / GPO3	Y3	O	**Suspend Status 1** (Rx94[4] = 0). Typically connected to the North Bridge to provide information on host clock status. Asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, or STD suspend states. Connect 10K PU to VSUS33.
SUSCLK	AB1	O	**Suspend Clock.** 32.768 KHz output clock for use by the North Bridge (e.g., VT8633 or VT8366) for DRAM refresh purposes. Stopped during Suspend-to-Disk and Soft-Off modes. Connect 10K PU to VSUS33.
CPUMISS / GPI17	Y1	I	**CPU Missing.** Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to the CPUMISS pin of the CPU socket. The state of this pin may be read in the SMBus 2 registers. This pin may be used as CPUMISS and GPI17 at the same time.
AOLGPI / GPI18 / THRM#	Y4	I	**Alert On LAN.** The state of this pin may be read in the SMBus 2 registers. This pin may be used as AOLGPI, GPI18 and THRM# all at the same time.

Resets, Clocks, and Power Status			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PWRGD	AF4	I	**Power Good.** Connected to the Power Good signal on the Power Supply. Internal logic powered by VBAT.
PWROK#	AE2	O	**Power OK.** Internal logic powered by VSUS33.
PCIRST#	R2	O	**PCI Reset.** Active low reset signal for the PCI bus. The VT8235 will assert this pin during power-up or from the control register.
OSC	AC12	I	**Oscillator.** 14.31818 MHz clock signal used by the internal Timer.
RTCX1	AD4	I	**RTC Crystal Input**: 32.768 KHz crystal or oscillator input. This input is used for the internal RTC and power-well power management logic and is powered by VBAT.
RTCX2	AF3	O	**RTC Crystal Output**: 32.768 KHz crystal output. Internal logic powered by VBAT.
TEST	AF9	I	**Test.**
TPO	U24	O	**Test Pin Output.** Output pin for test mode.

Power and Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCC33	(see pin list)	P	**I/O Power.** 3.3V ±5%
VCC	(see pin list)	P	**Core Power.** 2.5V ±5%. This supply is turned on only when the mechanical switch on the power supply is turned on and the PWRON signal is conditioned high. ***Note: The VT8235L core voltage is 2.5V so board designs that are intended to allow use of either VT8235 or VT8235L should take this difference into account and allow the core voltage to be selected as either 2.5V (for the VT8235) or 3.3V (for the VT8235L).***
GND	(see pin list)	P	**Ground.** Connect to primary motherboard ground plane.
VSUS33	AA4, AB4, AC4, AC5	P	**Suspend Power.** 3.3V ±5%. Always available unless the mechanical switch of the power supply is turned off. If the “soft-off” state is not implemented, then this pin can be connected to VCC33. Signals powered by or referenced to this plane are: PWRGD, RSMRST#, PWRBTN#, SMBCK1/2, SMBDT1/2, GPO0, SUSA# / GPO1, SUSB# / GPO2, SUSC#, SUSST1# / GPO3, SUSCLK / GPO4, GPI1, GPI2 / EXTSMI#, GPI3 / RING#, GPI4 / LID, GPI5 / BATLOW#, GPI6 / PME#, SMBALRT#
VSUS25	T4, U4	P	**Suspend Power.** 2.5V ±5%.
VSUSUSB	D15	P	**USB Suspend Power.** 2.5V ±5%.
VBAT	AE4	P	**RTC Battery.** Battery input for internal RTC (RTCX1, RTCX2)
VLVREF	J23	P	**V-Link Voltage Reference.** 0.9V ±5% for 4x transfers and 0.625V ±5% for 8x transfers.
VCCVK	(see pin list)	P	**V-Link Compensation Circuit Voltage.** 2.5V ±5%
MIIVCC	D11, D12, E11, E12	P	**LAN MII Power.** 3.3V ±5%.Power for LAN Media Independent Interface (interface to external PHY). Connect to VCC33 through a ferrite bead.
MIIVCC25	D13, E13	P	**LAN MII Suspend Power.** 2.5V ±5%.
RAMVCC	E7	P	**LAN RAM Power.** 2.5V ±5%. Power for LAN internal RAM. Connect to VCC through a ferrite bead.
RAMGND	E8	P	**LAN RAM Ground.** Connect to GND through a ferrite bead.
USBVCC	(see pin list)	P	**USB 2.0 Differential Output Power.** 3.3V ±5%. Power for USB differential outputs (USBP0+, P0–, P1+, P1–, P2+, P2–, P3+, P3–, P4+, P4–, P5+, P5–). Connect to VSUS33 through a ferrite bead.
USBGND	(see pin list)	P	**USB 2.0 Differential Output Ground.** Connect to GND through a ferrite bead.
VCCUPLL	A23, D22	P	**USB 2.0 PLL Analog Voltage.** 2.5V ±5%. Connect to VCC through a ferrite bead.
GNDUPLL	B23, E22	P	**USB 2.0 PLL Analog Ground.** Connect to GND through a ferrite bead.
PLLVCC	P22	P	**PLL Analog Power.** 2.5V ±5%. Connect to VCC through a ferrite bead.
PLLGND	P23	P	**PLL Analog Ground.** Connect to GND through a ferrite bead.
PDVREF	W22	P	**IDE Primary Data Channel Voltage Reference.** 0.9V†
SDVREF	AD17	P	**IDE Secondary Data Channel Voltage Reference.** 0.9V†

†Created by a resistive voltage divider of 1KΩ 1% to 3.3V and 383Ω 1% to ground (see Design Guide)

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the VT8235. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details).

Detailed register descriptions are provided in the following section of this document. All offset and default values are shown in hexadecimal unless otherwise indicated

Table 4. Memory Mapped Registers

FEC00000	APIC Index	(8-bit)
FEC00010	APIC Data	(32-bit)
FEC00020	APIC IRQ Pin Assertion	(8-bit)
FEC00040	APIC EOI	(8-bit)

"APIC" = "Advanced Programmable Interrupt Controller"

Table 5. Function Summary

Bus	Device	Func	Device ID	Function
0	16 (10h)	0	3038h	USB 1.1 UHCI Ports 0-1
0	16 (10h)	1	3038h	USB 1.1 UHCI Ports 2-3
0	16 (10h)	2	3038h	USB 1.1 UHCI Ports 4-5
0	16 (10h)	3	3038h	USB 2.0 EHCI Ports 0-5
0	17 (11h)	0	3074h	Bus Control & Power Mgmt
0	17 (11h)	1	0571h	IDE Controller
0	17 (11h)	5	3059h	AC97 Audio Codec Controller
0	17 (11h)	6	3068h	MC97 Modem Codec Ctrlr
0	18 (12h)	0	3043h	VIA LAN Controller

Table 6. System I/O Map

Port	Function	Actual Port Decoding
00-1F	Master DMA Controller	0000 0000 000x nnnn
20-3F	Master Interrupt Controller	0000 0000 001x xxxn
40-5F	Timer / Counter	0000 0000 010x xxnn
60-6F	Keyboard Controller	0000 0000 0110 xnxn
(60h)	KBC Data	0000 0000 0110 x0x0
(61h)	Misc Functions & Spkr Ctrl	0000 0000 0110 xxx1
(64h)	KBC Command / Status	0000 0000 0110 x1x0
70-77	RTC/CMOS/NMI-Disable	0000 0000 0111 0nnn
78-7F	-available for system use-	0000 0000 0111 1xxx
80	-reserved- (debug port)	0000 0000 1000 0000
81-8F	DMA Page Registers	0000 0000 1000 nnnn
90-91	-available for system use-	0000 0000 1001 000x
92	System Control	0000 0000 1001 0010
93-9F	-available for system use-	0000 0000 1001 nnnn
A0-BF	Slave Interrupt Controller	0000 0000 101x xxxn
C0-DF	Slave DMA Controller	0000 0000 110n nnnx
E0-FF	-available for system use-	0000 0000 111x xxxx
100-CF7	-available for system use*	
CF8-CFB	PCI Configuration Address	0000 1100 1111 10xx
CFC-CFF	PCI Configuration Data	0000 1100 1111 11xx
D00-FFFF	-available for system use-	

Table 7. Registers

Legacy I/O Registers

Port	Master DMA Controller Registers	Default	Acc
00	Channel 0 Base & Current Address		RW
01	Channel 0 Base & Current Count		RW
02	Channel 1 Base & Current Address		RW
03	Channel 1 Base & Current Count		RW
04	Channel 2 Base & Current Address		RW
05	Channel 2 Base & Current Count		RW
06	Channel 3 Base & Current Address		RW
07	Channel 3 Base & Current Count		RW
08	Status / Command		RW
09	Write Request		**WO**
0A	Write Single Mask		**WO**
0B	Write Mode		**WO**
0C	Clear Byte Pointer FF		**WO**
0D	Master Clear		**WO**
0E	Clear Mask		**WO**
0F	Read / Write Mask		RW

Port	Master Interrupt Controller Regs	Default	Acc
20	Master Interrupt Control	—	*
21	Master Interrupt Mask	—	*
20	Master Interrupt Control Shadow	—	**RW**
21	Master Interrupt Mask Shadow	—	**RW**

* RW if shadow registers are disabled

Port	Timer/Counter Registers	Default	Acc
40	Timer / Counter 0 Count		RW
41	Timer / Counter 1 Count		RW
42	Timer / Counter 2 Count		RW
43	Timer / Counter Control		**WO**

Port	Keyboard Controller Registers	Default	Acc
60	Keyboard Controller Data		RW
61	Misc Functions & Speaker Control		RW
64	Keyboard Ctrlr Command / Status		RW

Port	CMOS / RTC / NMI Registers	Default	Acc
70	CMOS Memory Address & NMI Disa		**WO**
71	CMOS Memory Data (128 bytes)		RW
74	CMOS Memory Address		RW
75	CMOS Memory Data (256 bytes)		RW

NMI Disable is port 70h (CMOS Memory Address) bit-7.
RTC control occurs via specific CMOS data locations (0-Dh).
Ports 74-75 may be used to access CMOS if the internal RTC is disabled.

Legacy I/O Registers (continued)

Port	DMA Page Registers	Default	Acc
87	DMA Page – DMA Channel 0		RW
83	DMA Page – DMA Channel 1		RW
81	DMA Page – DMA Channel 2		RW
82	DMA Page – DMA Channel 3		RW
8F	DMA Page – DMA Channel 4		RW
8B	DMA Page – DMA Channel 5		RW
89	DMA Page – DMA Channel 6		RW
8A	DMA Page – DMA Channel 7		RW

Port	System Control Registers	Default	Acc
92	System Control		RW

Port	Slave Interrupt Controller Regs	Default	Acc
A0	Slave Interrupt Control	—	*
A1	Slave Interrupt Mask	—	*
A0	Slave Interrupt Control Shadow	—	**RW**
A1	Slave Interrupt Mask Shadow	—	**RW**

* RW accessible if shadow registers are disabled

Port	Slave DMA Controller Registers	Default	Acc
C0	Channel 0 Base & Current Address		RW
C2	Channel 0 Base & Current Count		RW
C4	Channel 1 Base & Current Address		RW
C6	Channel 1 Base & Current Count		RW
C8	Channel 2 Base & Current Address		RW
CA	Channel 2 Base & Current Count		RW
CC	Channel 3 Base & Current Address		RW
CE	Channel 3 Base & Current Count		RW
D0	Status / Command		RW
D2	Write Request		**WO**
D4	Write Single Mask		**WO**
D6	Write Mode		**WO**
D8	Clear Byte Pointer FF		**WO**
DA	Master Clear		**WO**
DC	Clear Mask		**WO**
DE	Read / Write Mask		RW

Keyyboard / Mouse Wakeup Registers (I/O Space)

Port	KB / Mouse Wakeup Registers	Default	Acc
002E	Keyboard / Mouse Wakeup Index †	00	RW
002F	Keyboard / Mouse Wakeup Data †	00	RW

† Keyboard / Mouse Wakeup registers (index values E0-EF defined below) are accessible if Function 0 PCI Configuration register Rx51[1] = 1.

Keyboard / Mouse Wakeup Registers (Indexed via Port 2E/2F)

Offset	Reserved	Default	Acc
00-DF	-reserved-	—	RO

Offset	KB / Mouse Wakeup (Rx51[1]=1)	Default	Acc
E0	Keyboard / Mouse Wakeup Enable	**08**	**RW**
E1	Keyboard Wakeup Scan Code Set 0	**F0**	**RW**
E2	Keyboard Wakeup Scan Code Set 1	00	**RW**
E3	Keyboard Wakeup Scan Code Set 2	00	**RW**
E4	Keyboard Wakeup Scan Code Set 3	00	**RW**
E5	Keyboard Wakeup Scan Code Set 4	00	**RW**
E6	Keyboard Wakeup Scan Code Set 5	00	**RW**
E7	Keyboard Wakeup Scan Code Set 6	00	**RW**
E8	Keyboard Wakeup Scan Code Set 7	00	**RW**
E9	Mouse Wakeup Scan Code Set 1	**09**	**RW**
EA	Mouse Wakeup Scan Code Set 2	00	**RW**
EB	Mouse Wakeup Scan Code Mask	00	**RW**
EC-EF	-reserved-	—	RO

Game Port Registers (I/O Space)

Offset	Game Port (200-20F typical)	Default	Acc
0	-reserved-	00	—
1	Game Port Status		**RO**
1	Start One-Shot		**WO**
2-F	-reserved-	00	—

Memory Mapped Registers – IOAPIC

Address	APIC Index / Data	Default	Acc
FEC00000	APIC Register Index	00	RW
FEC00001-0F	-reserved-	00	—
FEC00010-13	APIC Register Data	0000 0000	RW
FEC00014-1F	-reserved-	00	—
FEC00020	APIC IRQ Pin Assertion	xx	**WO**
FEC00021-3F	-reserved-	00	—
FEC00040	APIC EOI	xx	**WO**
FEC00041-FF	-reserved-	00	—

Offset	APIC Registers	Default	Acc
0	APIC ID	0000 0000	RW
1	APIC Version	0017 8003	**RO**
2	APIC Arbitration	0000 0000	**RO**
3	Boot Configuration	0000 0000	RW
4-F	-reserved-	0000 0000	—
11-10	I/O Redirection– AIRQ0	xxx1xxxx xxxxxxxx	RW
13-12	I/O Redirection– AIRQ1	xxx1xxxx xxxxxxxx	RW
15-14	I/O Redirection– AIRQ2	xxx1xxxx xxxxxxxx	RW
17-16	I/O Redirection– AIRQ3	xxx1xxxx xxxxxxxx	RW
19-18	I/O Redirection– AIRQ4	xxx1xxxx xxxxxxxx	RW
1B-1A	I/O Redirection– AIRQ5	xxx1xxxx xxxxxxxx	RW
1D-1C	I/O Redirection– AIRQ6	xxx1xxxx xxxxxxxx	RW
1F-1E	I/O Redirection– AIRQ7	xxx1xxxx xxxxxxxx	RW
21-20	I/O Redirection– AIRQ8	xxx1xxxx xxxxxxxx	RW
23-20	I/O Redirection– AIRQ9	xxx1xxxx xxxxxxxx	RW
25-24	I/O Redirection– AIRQ10	xxx1xxxx xxxxxxxx	RW
27-26	I/O Redirection– AIRQ11	xxx1xxxx xxxxxxxx	RW
29-28	I/O Redirection– AIRQ12	xxx1xxxx xxxxxxxx	RW
2B-2A	I/O Redirection– AIRQ13	xxx1xxxx xxxxxxxx	RW
2D-2C	I/O Redirection– AIRQ14	xxx1xxxx xxxxxxxx	RW
2F-2E	I/O Redirection– AIRQ15	xxx1xxxx xxxxxxxx	RW
31-30	I/O Redirection– AIRQ16	xxx1xxxx xxxxxxxx	RW
33-32	I/O Redirection– AIRQ17	xxx1xxxx xxxxxxxx	RW
35-34	I/O Redirection– AIRQ18	xxx1xxxx xxxxxxxx	RW
37-36	I/O Redirection– AIRQ19	xxx1xxxx xxxxxxxx	RW
39-38	I/O Redirection– AIRQ20	xxx1xxxx xxxxxxxx	RW
3B-3A	I/O Redirection– AIRQ21	xxx1xxxx xxxxxxxx	RW
3D-3C	I/O Redirection– AIRQ22	xxx1xxxx xxxxxxxx	RW
3F-3E	I/O Redirection– AIRQ23	xxx1xxxx xxxxxxxx	RW
40-4F	-reserved-	0000 0000	—

Note: The "I/O Redirection" registers are 64-bit registers, so each uses two consecutive index locations, with the lower 32 bits at the even index and the upper 32 bits at the odd index.

Device 16 Function 0 Registers – USB 1.1 UHCI Ports 0-1

Configuration Space USB Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3038**	RO
5-4	Command	0000	**RW**
7-6	Status	**0210**	**WC**
8	Revision ID	**nn**	RO
9	Programming Interface	00	RO
A	Sub Class Code	**03**	RO
B	Base Class Code	**0C**	RO
C	-reserved-	00	—
D	Latency Timer	**16**	**RW**
E-1F	-reserved-	00	—
23-20	USB I/O Registers Base Port Address	**00000301**	**RW**
24-2B	-reserved-	00	—
2D-2C	Sub Vendor ID	**1106**	RO†
2F-2E	Sub Device ID	**3038**	RO†
30-33	-reserved-	00	—
34	Power Management Capabilities	**80**	RO
35-3B	-reserved-	00	—
3C	Interrupt Line	00	**RW**
3D	Interrupt Pin	**01**	RO
3E-3F	-reserved-	00	—

† RW if Rx42[4] = 1.

Configuration Space USB-Specific Registers

Offset	USB Control	Default	Acc
40	USB Miscellaneous Control 1	**40**	RW
41	USB Miscellaneous Control 2	**10**	RW
42	USB Miscellaneous Control 3	**03**	RW
43	USB Miscellaneous Control 4	00	RW
44-47	-reserved- (test, do not program)	00	**—**
48	USB Miscellaneous Control 5	00	RW
49	USB Miscellaneous Control 6	00	RW
4A	USB Miscellaneous Control 7	00	RW
4B-5F	-reserved-	00	—
60	USB Serial Bus Release Number	**10**	**RO**
61-83	-reserved-	00	—
84	PM Capability Status	00	RW
85-BF	-reserved-	00	—
C1-C0	USB Legacy Support	**2000**	RW
C2-FF	-reserved-	00	—

Memory Mapped I/O Registers – USB Controller

Offset	USB I/O Registers	Default	Acc
1-0	USB Command	0000	RW
3-2	USB Status	0000	**WC**
5-4	USB Interrupt Enable	0000	RW
7-6	Frame Number	0000	RW
B-8	Frame List Base Address	00000000	RW
C	Start Of Frame Modify	**40**	RW
11-10	Port 0 Status / Control	**0080**	**WC**
13-12	Port 1 Status / Control	**0080**	**WC**
14-1F	-reserved-	00	—

Device 16 Function 1 Registers – USB 1.1 UHCI Ports 2-3

Configuration Space USB Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3038**	RO
5-4	Command	0000	**RW**
7-6	Status	**0210**	**WC**
8	Revision ID	**nn**	RO
9	Programming Interface	00	RO
A	Sub Class Code	**03**	RO
B	Base Class Code	**0C**	RO
C	-reserved-	00	—
D	Latency Timer	**16**	**RW**
E-1F	-reserved-	00	—
23-20	USB I/O Registers Base Port Address	**00000301**	**RW**
24-2B	-reserved-	00	—
2D-2C	Sub Vendor ID	**1106**	RO†
2F-2E	Sub Device ID	**3038**	RO†
30-33	-reserved-	00	—
34	Power Management Capabilities	**80**	RO
35-3B	-reserved-	00	—
3C	Interrupt Line	00	**RW**
3D	Interrupt Pin	**02**	RO
3E-3F	-reserved-	00	—

† RW if Rx42[4] = 1.

Configuration Space USB-Specific Registers

Offset	USB Control	Default	Acc
40	USB Miscellaneous Control 1	**40**	RW
41	USB Miscellaneous Control 2	**10**	RW
42	USB Miscellaneous Control 3	**03**	RW
43	USB Miscellaneous Control 4	00	RW
44-47	-reserved- (test, do not program)	00	**—**
48	USB Miscellaneous Control 5	00	RW
49	USB Miscellaneous Control 6	00	RW
4A	USB Miscellaneous Control 7	00	RW
4B-5F	-reserved-	00	—
60	USB Serial Bus Release Number	**10**	**RO**
61-83	-reserved-	00	—
84	PM Capability Status	00	RW
85-BF	-reserved-	00	—
C1-C0	USB Legacy Support	**2000**	RW
C2-FF	-reserved-	00	—

Memory Mapped I/O Registers – USB Controller

Offset	USB I/O Registers	Default	Acc
1-0	USB Command	0000	RW
3-2	USB Status	0000	**WC**
5-4	USB Interrupt Enable	0000	RW
7-6	Frame Number	0000	RW
B-8	Frame List Base Address	00000000	RW
C	Start Of Frame Modify	**40**	RW
11-10	Port 0 Status / Control	**0080**	**WC**
13-12	Port 1 Status / Control	**0080**	**WC**
14-1F	-reserved-	00	—

Device 16 Function 2 Registers – USB 1.1 UHCI Ports 4-5

Configuration Space USB Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3038**	RO
5-4	Command	0000	**RW**
7-6	Status	**0210**	**WC**
8	Revision ID	**nn**	RO
9	Programming Interface	00	RO
A	Sub Class Code	**03**	RO
B	Base Class Code	**0C**	RO
C	-reserved-	00	—
D	Latency Timer	**16**	**RW**
E-1F	-reserved-	00	—
23-20	USB I/O Registers Base Port Address	**00000301**	**RW**
24-2B	-reserved-	00	—
2D-2C	Sub Vendor ID	**1106**	RO†
2F-2E	Sub Device ID	**3038**	RO†
30-33	-reserved-	00	—
34	Power Management Capabilities	**80**	RO
35-3B	-reserved-	00	—
3C	Interrupt Line	00	**RW**
3D	Interrupt Pin	**03**	RO
3E-3F	-reserved-	00	—

† RW if Rx42[4] = 1.

Configuration Space USB-Specific Registers

Offset	USB Control	Default	Acc
40	USB Miscellaneous Control 1	**40**	RW
41	USB Miscellaneous Control 2	**10**	RW
42	USB Miscellaneous Control 3	**03**	RW
43	USB Miscellaneous Control 4	00	RW
44-47	-reserved- (test, do not program)	00	**—**
48	USB Miscellaneous Control 5	00	RW
49	USB Miscellaneous Control 6	00	RW
4A	USB Miscellaneous Control 7	00	RW
4B-5F	-reserved-	00	—
60	USB Serial Bus Release Number	**10**	**RO**
61-83	-reserved-	00	—
84	PM Capability Status	00	RW
85-BF	-reserved-	00	—
C1-C0	USB Legacy Support	**2000**	RW
C2-FF	-reserved-	00	—

Memory Mapped I/O Registers – USB Controller

Offset	USB I/O Registers	Default	Acc
1-0	USB Command	0000	RW
3-2	USB Status	0000	**WC**
5-4	USB Interrupt Enable	0000	RW
7-6	Frame Number	0000	RW
B-8	Frame List Base Address	00000000	RW
C	Start Of Frame Modify	**40**	RW
11-10	Port 0 Status / Control	**0080**	**WC**
13-12	Port 1 Status / Control	**0080**	**WC**
14-1F	-reserved-	00	—

Device 16 Function 3 Registers – USB 2.0 EHCI Ports 0-5

Configuration Space USB Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3104**	RO
5-4	Command	0000	**RW**
7-6	Status	**0210**	**WC**
8	Revision ID	**nn**	RO
9	Programming Interface	**20**	RO
A	Sub Class Code	**03**	RO
B	Base Class Code	**0C**	RO
C	Cache Line Size	00	**RW**
D	Latency Timer	**16**	**RW**
E-F	-reserved-	00	—
13-10	EHCI Mem Mapped I/O Base Addr	0000 0000	**RW**
14-2B	-reserved-	00	—
2D-2C	Sub Vendor ID	**1106**	RO†
2F-2E	Sub Device ID	**3104**	RO†
30-33	-reserved-	00	—
34	Power Management Capabilities	**80**	RO
35-3B	-reserved-	00	—
3C	Interrupt Line	00	**RW**
3D	Interrupt Pin	**04**	RO
3E-3F	-reserved-	00	—

† RW if Rx42[4] = 1.

Configuration Space USB-Specific Registers

Offset	USB Control	Default	Acc
40	USB Miscellaneous Control 1	00	RW
41-47	-reserved- (Do Not Program)	00	—
48	USB Miscellaneous Control 5	**A0**	RW
49	USB Miscellaneous Control 6	**20**	RW
4A-4B	-reserved- (Do Not Program)	00	—
4C-4F	-reserved-	00	—
50-57	-reserved- (test, do not program)	00	**—**
58-5D	-reserved- (Do Not Program)	00	—
5E-5F	-reserved-	00	—
60	USB Serial Bus Release Number	**20**	**RO**
61	Frame Length Adjust	**20**	RW
63-62	Port Wake Capability	**0001**	RW
64-67	-reserved-	00	—
6B-68	Legacy Support Extended Capability	**0000 0001**	RW
6F-6C	Legacy Support Control / Status	0000 0000	RW
70-83	-reserved-	00	—
84	PM Capability Status	00	RW
85-FF	-reserved-	00	—

Memory Mapped I/O Registers – USB EHCI

Offset	EHCI Capabilities	Default	Acc
00	Capability Register Length	00	RW
01	-reserved-	00	—
03-02	Interface Version Number	**0100**	RO†
07-04	Structure Parameters	**0000 3206**	RO†
0B-08	Capability Parameters	**0000 6872**	RO†
0C-0F	-reserved-	00	—

† RW if Rx42[4] = 1.

Offset	Host Controller Operation	Default	Acc
13-10	USB Command	0000 0000	RW
17-14	USB Status	0000 0000	RW
1B-18	USB Interrupt Enable	0000 0000	RW
1F-1C	USB Frame Index	0000 0000	RW
23-20	4G Segment Selector	0000 0000	RW
27-24	Frame List Base Address	0000 0000	RW
2B-28	Next Asynchronous List Address	0000 0000	RW
2C-4F	-reserved-	00	—
53-50	Configured Flag Register	0000 0000	RW
57-54	Port 1 Status / Control	0000 0000	RW
5B-58	Port 2 Status / Control	0000 0000	RW
5C-FF	-reserved-	00	—

Device 17 Function 0 Registers – Bus Control & Power Management

Configuration Space Bus Control & PM Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3177**	RO
5-4	Command	**0087**	**RW**
7-6	Status	**0200**	**WC**
8	Revision ID	**nn**	RO
9	Programming Interface	00	RO
A	Sub Class Code	**01**	RO
B	Base Class Code	**06**	RO
C	-reserved- (cache line size)	00	—
D	-reserved- (latency timer)	00	—
E	Header Type	**80**	RO
F	Built In Self Test (BIST)	00	RO
10-27	-reserved- (base address registers)	00	—
28-2B	-reserved- (unassigned)	00	—
2D-2C	Sub Vendor ID	00	RO
2F-2E	Sub Device ID	00	RO
30-33	-reserved- (expan. ROM base addr)	00	—
34-3B	-reserved- (unassigned)	00	—
3C	-reserved- (interrupt line)	00	—
3D	-reserved- (interrupt pin)	00	—
3E	-reserved- (min gnt)	00	—
3F	-reserved- (max lat)	00	—

Configuration Space PCI-to-ISA Bridge-Specific Registers

Offset	ISA Bus Control	Default	Acc
40	ISA Bus Control	00	RW
41	BIOS ROM Decode Control	00	RW
42	Line Buffer Control	00	RW
43	Delay Transaction Control	00	RW
44-47	-reserved-	00	—
48	Read Pass Write Control	00	RW
49	CCA Control	00	RW
4A-4B	-reserved-	00	—

Offset	Miscellaneous Control	Default	Acc
4C	IDE Interrupt Routing	00	RW
4D	-reserved-	00	—
4E	Internal RTC Test Mode	00	RW
4F	PCI Bus & CPU Interface Control	00	RW

Offset	Function Control	Default	Acc
50	Function Control 1	**09**	RW
51	Function Control 2	**0D**	RW

Offset	Serial IRQ, LPC & PC/PCI Control	Default	Acc
52	Serial IRQ & LPC Control	00	RW
53	PC/PCI DMA Control	00	RW

Offset	Plug and Play Control	Default	Acc
54	PCI Interrupt Polarity	00	RW
55	PnP Routing for PCI INTA	00	RW
56	PnP Routing for PCI INTB-C	00	RW
57	PnP Routing for PCI INTD	00	RW

Offset	GPIO and Miscellaneous Control	Default	Acc
58	Miscellaneous Control 0	**40**	RW
59	Miscellaneous Control 1	00	RW
5A	DMA Bandwidth Control	00	RW
5B	Miscellaneous Control 2	00	RW

Offset	Programmable Chip Select Control	Default	Acc
5D-5C	PCS0# I/O Port Address	0000	RW
5F-5E	PCS1# I/O Port Address	0000	RW
61-60	PCS2# I/O Port Address	0000	RW
63-62	PCS3# I/O Port Address	0000	RW
64	PCS[1-0]# I/O Port Address Mask	00	RW
65	PCS[3-2]# I/O Port Address Mask	00	RW
66	Programmable Chip Select Control	00	RW
67	Output Control	**04**	RW
68-6B	-reserved-	00	—

Offset	Miscellaneous	Default	Acc
6C	ISA Positive Decoding Control 1	00	RW
6D	ISA Positive Decoding Control 2	00	RW
6E	ISA Positive Decoding Control 3	00	RW
6F	ISA Positive Decoding Control 4	00	RW
71-70	Sub Vendor ID Backdoor	00	RW
73-72	Sub Device ID Backdoor	00	RW
70-78	-reserved-	00	—
79	PnP IRQ/DRQ Test (do not prog)	00	RW
7A	IDE / USB Test (do not program)	00	RW
7B	PLL Test (do not program)	00	RW
7C	I/O Pad Control	00	RW
7D-7F	-reserved-	00	—

Configuration Space Power Management Registers

Offset	Power Management	Default	Acc
80	General Configuration 0	00	RW
81	General Configuration 1	**04**	RW
82	ACPI Interrupt Select	00	RW
83	-reserved-	00	—
85-84	Primary Interrupt Channel	0000	RW
87-86	Secondary Interrupt Channel	0000	RW
8B-88	Power Mgmt I/O Base (256 Bytes)	**0000 0001**	RW
8C	Host Bus Power Mgmt Control	00	RW
8D	Throttle / Clock Stop Control	00	RW
8E-8F	-reserved-	00	—
93-90	GP Timer Control	0000 0000	RW
94	Power Well Control	00	RW
95	Miscellaneous Control	00	RW
96	Power On / Reset Control	00	RW
97	-reserved-	00	—
98	GP2 / GP3 Timer Control	00	RW
99	GP2 Timer	00	RW
9A	GP3 Timer	00	RW
9B-A0	-reserved-	00	—
A1	Write value for Offset 9 (Prog Intfc)	00	**WO**
A2	Write value for Offset A (Sub Class)	00	**WO**
A3	Write value for Offset B (Base Class)	00	**WO**
A4-BF	-reserved-	00	—
C3-C0	Power Management Capability	**0002 0001**	**RO**
C7-C4	Power Management Capability CSR	**0000 0000**	RW
C8-CF	-reserved-	00	—

Configuration Space SMBus Registers

Offset	System Management Bus	Default	Acc
D1-D0	SMBus I/O Base (16 Bytes)	**0001**	RW
D2	SMBus Host Configuration	00	RW
D3	SMBus Host Slave Command	00	RW
D4	SMBus Slave Address Shadow Port 1	00	RW
D5	SMBus Slave Address Shadow Port 2	00	RW
D6	SMBus Revision ID	**nn**	**RO**
D7-DF	-reserved-	00	—

Configuration Space General Purpose I/O Registers

Offset	General Purpose I/O	Default	Acc
E0	GPI Inversion Control	00	RW
E1	GPI SCI / SMI Select	00	RW
E2-E3	-reserved-	00	—
E4	GPO Pin Select	00	RW
E5	GPIO I/O Select 1	00	RW
E6	GPIO I/O Select 2	00	RW
E7	GPO Output Type	00	RW
E8-FF	-reserved-	00	—

I/O Space Power Management Registers

Offset	Basic Control / Status Registers	Default	Acc
1-0	Power Management Status	0000	**WC**
3-2	Power Management Enable	0000	RW
5-4	Power Management Control	0000	RW
6-7	-reserved-	00	—
B-8	Power Management Timer	0000 0000	RW
C-F	-reserved-	00	—

Offset	Processor Registers	Default	Acc
13-10	Processor and PCI Bus Control	0000 0000	RW
14	Processor LVL2	00	**RO**
15	Processor LVL3	00	**RO**
16-1F	-reserved-	00	—

Offset	General Purpose Registers	Default	Acc
21-20	General Purpose Status	0000	**WC**
23-22	General Purpose SCI Enable	0000	RW
25-24	General Purpose SMI Enable	0000	RW
26-27	-reserved-	00	—

Offset	Generic Registers	Default	Acc
29-28	Global Status	0000	**WC**
2B-2A	Global Enable	0000	RW
2D-2C	Global Control	**0010**	RW
2E	-reserved-	00	—
2F	SMI Command	00	RW
33-30	Primary Activity Detect Status	0000 0000	**WC**
37-34	Primary Activity Detect Enable	0000 0000	RW
3B-38	GP Timer Reload Enable	0000 0000	RW
3C-3F	-reserved-	00	—

Offset	General Purpose I/O Registers	Default	Acc
40	Extended I/O Trap Status	00	**WC**
41	-reserved-	00	—
42	Extended I/O Trap Enable	00	RW
43-44	-reserved-	00	—
45	SMI / IRQ / Resume Status	00	**RO**
46-47	-reserved-	00	—
4B-48	GPI Port Input Value	**input**	**RO**
4F-4C	GPO Port Output Value	**FFFFCFFF**	RW
50	GPI Pin Change Status	00	RW
51	-reserved-	00	—
52	GPI Pin Change SCI/SMI Select	00	RW
53-57	-reserved-	00	—
59-58	I/O Trap PCI I/O Address	0000	**RO**
5A	I/O Trap PCI Command / Byte Ena	00	**RO**
5B	-reserved-	00	—
5C	CPU Performance Control	00	RW
5D-FF	-reserved-	00	—

I/O Space System Management Bus Registers

Offset	System Management Bus	Default	Acc
0	SMBus Host Status	00	**WC**
1	SMBus Slave Status	00	RW
2	SMBus Host Control	00	RW
3	SMBus Host Command	00	RW
4	SMBus Host Address	00	RW
5	SMBus Host Data 0	00	RW
6	SMBus Host Data 1	00	RW
7	SMBus Block Data	00	RW
8	SMBus Slave Control	00	RW
9	SMBus Shadow Command	00	**RO**
A-B	SMBus Slave Event	0000	RW
C-D	SMBus Slave Data	0000	**RO**
E	-reserved-	00	—
F	SMBus GPIO Slave Address	00	RW

System Management Bus Command Codes

Code	System Management Bus	Default	Acc
00	SMBus GPIO Slave Input Data	—	**RO**
01	SMBus GPIO Slave Output Data	00	RW
02	SMBus GPIO Slave Polarity Inversion	**F0**	RW
03	SMBus GPIO Slave I/O Configuration	**FF**	RW

Device 17 Function 1 Registers – IDE Controller

Configuration Space IDE Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**0571**	RO
5-4	Command	**0080**	RO
7-6	Status	**0290**	**RW**
8	Revision ID	**nn**	RO
9	Programming Interface	**85**	**RW**
A	Sub Class Code	**01**	RO
B	Base Class Code	**01**	RO
C-F	-reserved-	00	—
13-10	Base Address – Pri Data / Command	**000001F1**	**RW**
17-14	Base Address – Pri Control / Status	**000003F5**	**RW**
1B-18	Base Address – Sec Data / Command	**00000171**	**RW**
1F-1C	Base Address – Sec Control / Status	**00000375**	**RW**
23-20	Base Address – Bus Master Control	**0000CC01**	**RW**
24-2B	-reserved- (unassigned)	00	—
2D-2C	Sub Vendor ID	0000	RO
2F-2E	Sub Device ID	0000	RO
30-33	-reserved- (expan ROM base addr)	00	—
34	Capability Pointer	**C0**	RO
35-3B	-reserved- (unassigned)	00	—
3C	Interrupt Line	**0E**	RO
3D	Interrupt Pin	00	RO
3E	Minimum Grant	00	RO
3F	Maximum Latency	00	RO

Configuration Space IDE-Specific Registers

Offset	Configuration Space IDE Registers	Default	Acc
40	IDE Chip Enable	00	RW
41	IDE Configuration I	00	RW
42	IDE Configuration II	00	RW
43	IDE FIFO Configuration	**0A**	RW
44	IDE Miscellaneous Control 1	**08**	RW
45	IDE Miscellaneous Control 2	**10**	RW
46	IDE Miscellaneous Control 3	**C0**	RW
4B-48	IDE Drive Timing Control	**A8A8A8A8**	RW
4C	IDE Address Setup Time	**FF**	RW
4D	-reserved- (do not program)	00	RW
4E	Sec Non-1F0 Port Access Timing	**B6**	RW
4F	Pri Non-1F0 Port Access Timing	**B6**	RW

Configuration Space IDE-Specific Registers (continued)

Offset	Configuration Space IDE Registers	Default	Acc
53-50	UltraDMA Extended Timing Control	**07070707**	RW
54	UltraDMA FIFO Control	**04**	RW
55	IDE Clock Gating	00	RW
56-5F	-reserved-	00	—
61-60	IDE Primary Sector Size	**0200**	RW
62-67	-reserved-	00	—
69-68	IDE Secondary Sector Size	**0200**	RW
69-6F	-reserved-	00	—
70	IDE Primary Status	00	RW
71	IDE Primary Interrupt Control	**01**	RW
72-77	-reserved-	00	—
78	IDE Secondary Status	00	RW
79	IDE Secondary Interrupt Control	**01**	RW
7A-7F	-reserved-	00	—
83-80	IDE Primary S/G Descriptor Address	0000 0000	RW
84-87	-reserved-	00	—
8B-88	IDE Secondary S/G Descriptor Addr	0000 0000	RW
8C-BF	-reserved-	00	—
C3-C0	Power Management Capabilities	**0002 0001**	**RO**
C7-C4	Power State	0000 0000	RW
C8-CF	-reserved-	00	—

Offset	IDE Back Door Registers	Default	Acc
D0	Back Door – Revision ID	**06**	RW
D1	-reserved-	00	—
D3-D2	Back Door – Device ID	**0571**	RW
D5-D4	Back Door – Sub Vender ID	0000	RW
D7-D6	Back Door – Sub Device ID	0000	RW
D8-F5	-reserved-	00	—
F6	IDE New Revision ID	**07**	**RO**
F7-FF	-reserved-	00	—

I/O Registers – IDE Controller (SFF 8038 v1.0 Compliant

Offset	IDE I/O Registers	Default	Acc
0	Primary Channel Command	00	RW
1	-reserved-	00	—
2	Primary Channel Status	00	**WC**
3	-reserved-	00	—
4-7	Primary Channel PRD Table Addr	00	RW
8	Secondary Channel Command	00	RW
9	-reserved-	00	—
A	Secondary Channel Status	00	**WC**
B	-reserved-	00	—
C-F	Secondary Channel PRD Table Addr	00	RW

Device 17 Function 5 & 6 Registers – AC/MC97 Codecs

Function 5 Configuration Space AC97 Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3059**	RO
5-4	Command	0000	**RW**
7-6	Status	**0210**	RO
8	Revision ID	**50**	RO
9	Programming Interface	00	RO
A	Sub Class Code	**01**	RO
B	Base Class Code	**04**	RO
C-F	-reserved-	00	—
13-10	Base Address 0 - SGD Control/Status	**0000 0001**	**RW**
17-14	Base Address 1 (reserved)	0000 0000	—
1B-18	Base Address 2 (reserved)	0000 0000	—
1F-1C	Base Address 3 (reserved)	0000 0000	—
23-20	Base Address 4 (reserved)	0000 0000	—
27-24	Base Address 5 (reserved)	0000 0000	—
28-29	-reserved-	00	—
2F-2C	Subsystem ID / SubVendor ID	0000 0000	**RW**
33-30	Expansion ROM (reserved)	0000 0000	—
34	Capture Pointer	**C0**	**RW**
35-3B	-reserved-	00	—
3C	Interrupt Line	00	**RW**
3D	Interrupt Pin	**03**	RO
3E	Minimum Grant	00	RO
3F	Maximum Latency	00	RO

Function 6 Configuration Space MC97 Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3068**	RO
5-4	Command	0000	**RW**
7-6	Status	**0200**	RO
8	Revision ID	**70**	RO
9	Programming Interface	00	RO
A	Sub Class Code	**80**	RO
B	Base Class Code	**07**	RO
C-F	-reserved-	00	—
13-10	Base Address 0 - SGD Control/Status	**0000 0001**	**RW**
17-14	Base Address 1 (reserved)	0000 0000	—
1B-18	Base Address 2 (reserved)	0000 0000	—
1F-1C	Base Address 3 (reserved)	0000 0000	—
23-20	Base Address 4 (reserved)	0000 0000	—
27-24	Base Address 5 (reserved)	0000 0000	—
28-29	-reserved-	00	—
2F-2C	Subsystem ID / SubVendor ID	0000 0000	**RW**
33-30	Expansion ROM (reserved)	0000 0000	—
34	Capture Pointer	**D0**	**RW**
35-3B	-reserved-	00	—
3C	Interrupt Line	00	**RW**
3D	Interrupt Pin	**03**	RO
3E	Minimum Grant	00	RO
3F	Maximum Latency	00	RO

Configuration Space Audio Codec-Specific Registers

Offset	Audio Codec Link Control	Default	Acc
40	AC-Link Interface Status	00	**RO**
41	AC-Link Interface Control	00	RW
42	Function Enable	00	RW
43	-reserved-	00	—
44	MC97 Interface Control	00	**RO**
45-47	-reserved-	00	—
48	Value Change Rate Control	00	RW
49	S/PDIF Control	00	RW
4A-BF	-reserved-	00	—
C3-C0	Power Management Capability	**0002 0001**	**RO**
C7-C4	Power State	0000 0000	RW
C8-FF	-reserved-	00	—

Configuration Space Modem Codec-Specific Registers

Offset	Modem Codec Link Control	Default	Acc
40	AC-Link Interface Status	00	**RO**
41	AC-Link Interface Control	00	RW
42	Function Enable	00	**RO**
43	-reserved-	00	—
44	MC97 Interface Control	00	RW
45-47	-reserved-	00	—
48	Value Change Rate Control	00	**RO**
49	S/PDIF Control	00	**RO**
4A-CF	-reserved-	00	—
D3-D0	Power Management Capability	**0002 0001**	**RO**
D7-D4	Power State	0000 0000	RW
D8-FF	-reserved-	00	—

Function 5 I/O Base 0 Registers – AC97 Audio S/G DMA

Offset	AC97 SGD I/O Registers	Default	Acc
x0	SGD Channel x Status	00	**WC**
x1	SGD Channel x Control	00	RW
x2	SGD Channel x Left Volume	**3F**	RW
x3	SGD Channel x Right Volume	**3F**	RW
x7-x4	SGD Channel x Table Pointer Base SGD Channel x Current Address	0000 0000	WR RD
xB-x8	Stop Index / Data Type / Sample Rate	**FF0F FFFF**	RW
xF-xC	SGD Channel x Current Count	0000 0000	**RO**
40	SGD 3D Channel Status	00	**WC**
41	SGD 3D Channel Control	00	RW
42	SGD 3D Channel Format	00	RW
43	SGD 3D Channel Scratch	00	RW
47-44	SGD 3D Channel Table Pointer Base SGD 3D Channel Current Address	0000 0000	WR RD
4B-48	SGD 3D Channel Slot Select	**FF00 0000**	RW
4F-4C	SGD 3D Channel Current Count	0000 0000	**RO**
50-5F	-reserved-	00	—
60	SGD Write Channel 0 Status	00	**WC**
61	SGD Write Channel 0 Control	00	RW
62	SGD Write Channel 0 Format	00	RW
63	SGD Write Channel 0 Select	00	RW
67-64	SGD Write Channel 0 Table Ptr Base SGD Write Channel 0 Current Addr	0000 0000	WR RD
6B-68	SGD Write Channel 0 Stop Index	**FF00 0000**	RW
6F-6C	SGD Write Channel 0 Current Count	0000 0000	**RO**
70	SGD Write Channel 1 Status	00	**WC**
71	SGD Write Channel 1 Control	00	RW
72	SGD Write Channel 1 Format	00	RW
73	SGD Write Channel 1 Select	00	RW
77-74	SGD Write Channel 1 Table Ptr Base SGD Write Channel 1 Current Addr	0000 0000	WR RD
7B-78	SGD Write Channel 1 Stop Index	**FF00 0000**	RW
7F-7C	SGD Write Channel 1 Current Count	0000 0000	**RO**

Offset	AC97 / Audio Codec I/O Registers	Default	Acc
83-80	AC97 Controller Command / Status	0000 0000	RW
87-84	SGD Global IRQ Shadow	0000 0000	**RO**
8B-88	Modem Codec GPI Intr Status / GPIO	0000 0000	**RO**
8F-8C	Modem Codec GPI Interrupt Enable	0000 0000	**RO**
90-9F	Shadow PCI Config Registers 40-4F	n/a	**RO**
A0-FF	-reserved-	00	—

Function 6 I/O Base 0 Registers – MC97 Modem S/G DMA

Offset	MC97 SGD I/O Registers	Default	Acc
0-7	-reserved-	00	—
8-F	-reserved-	00	—
10-17	-reserved-	00	—
18-1F	-reserved-	00	—
20-27	-reserved-	00	—
28-2F	-reserved-	00	—
30-37	-reserved-	00	—
38-3F	-reserved-	00	—
40	SGD Read Channel Status	00	**WC**
41	SGD Read Channel Control	00	RW
42	SGD Read Channel Type	00	RW
43	-reserved-	00	—
47-44	SGD Read Chan Table Pointer Base SGD Read Channel Current Address	0000 0000	WR RD
4B-48	-reserved- (Test)	0000 0000	**RO**
4F-4C	SGD Read Channel Current Count	0000 0000	**RO**
50	SGD Write Channel Status	00	**WC**
51	SGD Write Channel Control	00	RW
52	SGD Write Channel Type	00	RW
53	-reserved-	00	—
57-54	SGD Write Channel Table Ptr Base SGD Write Channel Current Address	0000 0000	WR RD
5B-58	Reserved (Test)	0000 0000	**RO**
5F-5C	SGD Write Channel Current Count	0000 0000	**RO**
60-7F	-reserved-	00	—

Offset	AC97 / Modem Codec I/O Registers	Default	Acc
83-80	AC97 Controller Command / Status	0000 0000	RW
87-84	SGD Global IRQ Shadow	0000 0000	**RO**
8B-88	Modem Codec GPI Intr Status / GPIO	0000 0000	**WC**
8F-8C	Modem Codec GPI Interrupt Enable	0000 0000	RW
90-9F	Shadow PCI Config Registers 40-4F	n/a	**RO**
A0-FF	-reserved-	00	—

Device 18 Function 0 Registers - LAN

Configuration Space LAN Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3065**	RO
5-4	Command	0000	RO
7-6	Status	**0470**	**WC**
8	Revision ID	**40**	RO
9	Programming Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	00	RO
C	Cache Line Size	00	**RW**
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	BIST	00	RO
13-10	I/O Base Address	0000 0000	RW
17-14	Memory Base Address	0000 0000	RW
18-27	-reserved-	00	—
2B-28	Card Bus CIS Pointer	0000 0000	RW
2C-2F	-reserved-	00	—
33-30	Expansion ROM Base Address	0000 0000	RW
34	Capabilities Offset	**40**	**RO**
35-3C	-reserved-	00	—
3D	Interrupt Pin	**01**	**RO**
3E-3F	-reserved-	00	—

Configuration Space LAN Device Specific Registers

Offset	Power Management	Default	Acc
40	Capability ID	**01**	**RO**
41	Next Item Pointer	00	**RO**
43-42	Power Management Configuration	**0002**	**RO**
47-44	Power Management Control / Status	0000 0000	**WC**
48-FF	-reserved-	00	—

I/O Space LAN Registers

Offset	Power Management	Default	Acc
5-0	Ethernet Address		RW
6	Receive Control	00	RW
7	Transmit Control	**08**	RW
8	Command 0	00	RW
9	Command 1	00	RW
A-B	-reserved-	00	—
C	Interrupt Status 0	00	RW
D	Interrupt Status 1	00	RW
E	Interrupt Mask 0	00	RW
F	Interrupt Mask 1	00	RW
17-10	Multicast Address		RW
1B-18	Receive Address		RW
1F-1C	Transmit Address		RW
23-20	Receive Status	0000 0000	RW
27-24	Receive Data Buffer Control	0000 0000	**RO**
2B-28	Receive Data Buffer Start Address		**RO**
2F-2C	Receive Data Buffer Branch Address		**RO**
30-3F	-reserved-	00	—
43-40	Transmit Status	0000 0000	RW
47-44	Transmit Data Buffer Control	0000 0000	**RO**
4B-48	Transmit Data Buffer Start Address		**RO**
4F-4C	Transmit Data Buffer Branch Addr		**RO**
50-6B	-reserved-	00	—
6C	PHY Address	**01**	RW
6D	MII Status	**13**	RW
6E	Buffer Control 0	00	RW
6F	Buffer Control 1	00	RW
70	MII Management Port Command	00	RW
71	MII Management Port Address	**81**	RW
73-72	PHY Data	0000	**RW**
74	EEPROM Command / Status	00	RW
75-77	-reserved-	00	—
78	EEPROM Control	00	RW

I/O Space LAN Registers (continued)

Offset	Power Management	Default	Acc
79	Configuration 1	00	RW
7A	Configuration 2	00	RW
7B	Configuration 3	00	RW
7C-7F	-reserved-	00	—
80	Miscellaneous 1	00	RW
81	Miscellaneous 2	00	RW
82	-reserved-	00	—
83	Sticky Hardware Control	00	RW
84	MII Interrupt Status	00	**WC**
85	-reserved-	00	—
86	MII Interrupt Mask	00	RW
87-8B	-reserved-	00	—
8D-8C	Flash Address	0000	RW
8E	-reserved-	00	—
8F	Flash Write Data Output	00	RW
90	Flash Read / Write Command	00	RW
91	Flash Write Data Input	00	**RO**
92	-reserved-	00	—
93	Flash Checksum	00	RW
95-94	Suspend Mode MII Address	0000	RW
96	Suspend Mode PHY Address	00	RW
97	-reserved-	00	—
99-98	Pause Timer	0000	RW
9A	Pause Status	00	RW
9B	-reserved-	00	—
9D-9C	Soft Timer 0	0000	RW
9F-9E	Soft Timer 1	0000	RW
A0/A4	Wake On LAN Control Set / Clear	00 / 00	RW
A1/A5	Power Configuration Set / Clear	00 / 00	RW
A2/A6	-reserved- (do not program)	00 / 00	—
A3/A7	Wake On LAN Config Set / Clear	00 / 00	RW
A8-AF	-reserved-	00	—
B3-B0	Pattern CRC 0	0000 0000	RW
B7-B4	Pattern CRC 1	0000 0000	RW
BB-B8	Pattern CRC 2	0000 0000	RW
BF-BC	Pattern CRC 3	0000 0000	RW
CF-C0	Byte Mask 0	0000 0000	RW
DF-D0	Byte Mask 1	0000 0000	RW
EF-E0	Byte Mask 2	0000 0000	RW
FF-F0	Byte Mask 3	0000 0000	RW

Register Descriptions

Legacy I/O Ports

This group of registers includes the DMA Controllers, Interrupt Controllers, and Timer/Counters as well as a number of miscellaneous ports originally implemented using discrete logic on original PC/AT motherboards. All of the registers listed are integrated on-chip. These registers are implemented in a precise manner for backwards compatibility with previous generations of PC hardware. These registers are listed for information purposes only. Detailed descriptions of the actions and programming of these registers are included in numerous industry publications (duplication of that information here is beyond the scope of this document). All of these registers reside in I/O space.

Port 61 - Misc Functions & Speaker Control .... RW

- **7-6 Reserved** .... always reads 0
- **5 Timer/Counter 2 Output** .... RO
  This bit reflects the output of Timer/Counter 2 without any synchronization.
- **4 Refresh Detected** .... RO
  This bit toggles on every rising edge of the ISA bus REFRESH# signal.
- **3-2 Reserved** .... RW, default=0
- **1 Speaker Enable** .... RW
  - 0 Disable .... default
  - 1 Enable Timer/Ctr 2 output to drive SPKR pin
- **0 Timer/Counter 2 Enable** .... RW
  - 0 Disable .... default
  - 1 Enable Timer/Counter 2

Port 92h - System Control .... RW

- **7-6 Hard Disk Activity LED Status**
  - 0 Off .... default
  - 1-3 On
- **5-4 Reserved** .... always reads 0
- **3 Power-On Password Bytes Inaccessable** ... default=0
- **2 Reserved** .... always reads 0
- **1 A20 Address Line Enable**
  - 0 A20 disabled / forced 0 (real mode) ...... default
  - 1 A20 address line enabled
- **0 High Speed Reset**
  - 0 Normal
  - 1 Briefly pulse system reset to switch from protected mode to real mode

Keyboard Controller I/O Registers

The keyboard controller handles the keyboard and mouse interfaces. Two ports are used: port 60 and port 64. Reads from port 64 return a status byte. Writes to port 64h are command codes (see command code list following the register descriptions). Input and output data is transferred via port 60.

A "Control" register is also available. It is accessable by writing commands 20h / 60h to the command port (port 64h); The control byte is written by first sending 60h to the command port, then sending the control byte value. The control register may be read by sending a command of 20h to port 64h, waiting for "Output Buffer Full" status = 1, then reading the control byte value from port 60h.

Traditional (non-integrated) keyboard controllers have an "Input Port" and an "Output Port" that control pins dedicated to specific functions. In the integrated version, connections are hard wired as listed below. Outputs are "open-collector" so to allow input on one of these pins, the output value for that pin would be set high (non-driving) and the desired input value read on the input port. These ports are defined as follows:

Bit	Input Port
0	Keyboard Data In
1	Mouse Data In

Bit	Output Port
0	System Reset (1 = Execute Reset)
1	Gaste A20 (1 = A20 Enabled)
2	Mouse Data Out
3	Mouse Clock Out
6	Keyboard Clock Out
7	Keyboard Data Out

Bit	Test Port
0	Keyboard Clock In
1	Mouse Clock In

Hardwired Internal Connections

Keyboard Data Out (Open Collector) <=> Keyboard Data In
Keyboard Clock Out (Open Collector) <=> Keyboard Clk In

Mouse Data Out (Open Collector) <=> Mouse Data In
Mouse Clock Out (Open Collector) <=> Mouse Clock In

Keyboard OBF Interrupt => IRQ1
Mouse OBF Interrupt => IRQ12

Input / Output / Test Port Command Codes

C0h transfers input port data to the output buffer.
D0h copies output port values to the output buffer.
E0h transfers test input port data to the output buffer.

The above definitions are provided for reference only as actual keyboard and mouse control is no longer performed bit-by bit using the above ports but controlled directly by keyboard / mouse controller internal logic. Data is sent and received using the command codes listed on the following page.

Port 60 - Keyboard Controller Input Buffer .... WO

Only write to port 60h if port 64h bit-1 = 0 (1=full).

Port 60 - Keyboard Controller Output Buffer .... RO

Only read from port 60h if port 64h bit-0 = 1 (0=empty).

Port 64 - Keyboard / Mouse Status .... RO

7 Parity Error
- 0 No parity error (odd parity received) ..... default
- 1 Even parity occurred on last byte received from keyboard / mouse

6 General Receive / Transmit Timeout
- 0 No error .... default
- 1 Error

5 Mouse Output Buffer Full
- 0 Mouse output buffer empty.................... default
- 1 Mouse output buffer holds mouse data

4 Keylock Status
- 0 Locked
- 1 Free

3 Command / Data
- 0 Last write was data write .... default
- 1 Last write was command write

2 System Flag
- 0 Power-On Default................................. default
- 1 Self Test Successful

1 Input Buffer Full
- 0 Input Buffer Empty............................... default
- 1 Input Buffer Full

0 Keyboard Output Buffer Full
- 0 Keyboard Output Buffer Empty .... default
- 1 Keyboard Output Buffer Full

KBC Control Register ....(R/W via Commands 20h/60h)

7 Reserved .... always reads 0

6 PC Compatibility
- 0 Disable scan conversion
- 1 Convert scan codes to PC format; convert 2-byte break sequences to 1-byte PC-compatible break codes .... default

5 Mouse Interface
- 0 Enable .... default
- 1 Disable

4 Keyboard Interface
- 0 Enable .... default
- 1 Disable

3 Reserved .... always reads 0

2 System Flag .... default=0
This bit may be read back as status register bit-2

1 Mouse Interrupts
- 0 Disable... default
- 1 Enable - Generate interrupt on IRQ12 when mouse data comes into output buffer

0 Keyboard Interrupts
- 0 Disable... default
- 1 Enable - Generate interrupt on IRQ1 when output buffer has been written.

Port 64 - Keyboard / Mouse Command.......................... WO

This port is used to send commands to the keyboard / mouse controller. The command codes recognized by the VT8235 are listed in the table below.

Table 8. Keyboard Controller Command Codes

Code	Keyboard Command Code Description
20h	Read Control Byte (next byte is Control Byte)
21-3Fh	Read SRAM Data (next byte is Data Byte)
60h	Write Control Byte (next byte is Control Byte)
61-7Fh	Write SRAM Data (next byte is Data Byte)
A1h	Output Keyboard Controller Version #
A4h	Test if Password is installed (always returns F1h to indicate not installed)
A7h	Disable Mouse Interface
A8h	Enable Mouse Interface
A9h	Mouse Interface Test (puts test results in port 60h) (value: 0=OK, 1=clk stuck low, 2=clk stuck high, 3=data stuck lo, 4=data stuck hi, FF=general error)
AAh	KBC self test (returns 55h if OK, FCh if not)
ABh	Keyboard Interface Test (see A9h Mouse Test)
ADh	Disable Keyboard Interface
AEh	Enable Keyboard Interface
AFh	Return Version #
C0h	Read Input Port (read input data to output buffer)
C1h	Poll Input Port (read Mouse Data In continuously to status bit 5
C8h	Unblock Mouse Output (use before D1 to change active mode)
C9h	Reblock Mouse Output (protection mechanism for D1)
CAh	Read Mode (output KBC mode info to port 60 output buffer: bit-0=0 if ISA, 1 if PS/2)
D0h	Read Output Port (copy output port values to port 60)
D1h	Write Output Port (data byte following is written to keyboard output port as if it came from keyboard)
D2h	Write Keyboard Output Buffer & clear status bit-5 (write following byte to keyboard)
D3h	Write Mouse Output Buffer & set status bit-5 (write following byte to mouse; put value in mouse input buffer so it appears to have come from the mouse)
D4h	Write Mouse (write following byte to mouse)
E0h	Read Keyboard Clock In and Mouse Clock In (return in bits 0-1 respectively of response byte)
Exh	Set Mouse Clock Out per command bit 3 Set Mouse Data Out per command bit 2 Set Gate A20 per command bit 1
Fxh	Pulse Mouse Clock Out low for 6usec per cmd bit 3 Pulse Mouse Data Out low for 6usec per cmd bit 2 Pulse Gate A20 low for 6usec per command bit 1 Pulse System Reset low for 6usec per cmd bit 0

All other codes not listed are undefined.

DMA Controller I/O Registers

Ports 00-0F - Master DMA Controller

Channels 0-3 of the Master DMA Controller control System DMA Channels 0-3. There are 16 Master DMA Controller registers:

I/O Address Bits 15-0	Register Name	
0000 0000 000x 0000	**Ch 0 Base / Current Address**	**RW**
0000 0000 000x 0001	**Ch 0 Base / Current Count**	**RW**
0000 0000 000x 0010	**Ch 1 Base / Current Address**	**RW**
0000 0000 000x 0011	**Ch 1 Base / Current Count**	**RW**
0000 0000 000x 0100	**Ch 2 Base / Current Address**	**RW**
0000 0000 000x 0101	**Ch 2 Base / Current Count**	**RW**
0000 0000 000x 0110	**Ch 3 Base / Current Address**	**RW**
0000 0000 000x 0111	**Ch 3 Base / Current Count**	**RW**
0000 0000 000x 1000	**Status / Command**	**RW**
0000 0000 000x 1001	**Write Request**	**WO**
0000 0000 000x 1010	**Write Single Mask**	**WO**
0000 0000 000x 1011	**Write Mode**	**WO**
0000 0000 000x 1100	**Clear Byte Pointer F/F**	**WO**
0000 0000 000x 1101	**Master Clear**	**WO**
0000 0000 000x 1110	**Clear Mask**	**WO**
0000 0000 000x 1111	**R/W All Mask Bits**	**RW**

Ports C0-DF - Slave DMA Controller

Channels 0-3 of the Slave DMA Controller control System DMA Channels 4-7. There are 16 Slave DMA Controller registers:

I/O Address Bits 15-0	Register Name	
0000 0000 1100 000x	**Ch 4 Base / Current Address**	**RW**
0000 0000 1100 001x	**Ch 4 Base / Current Count**	**RW**
0000 0000 1100 010x	**Ch 5 Base / Current Address**	**RW**
0000 0000 1100 011x	**Ch 5 Base / Current Count**	**RW**
0000 0000 1100 100x	**Ch 6 Base / Current Address**	**RW**
0000 0000 1100 101x	**Ch 6 Base / Current Count**	**RW**
0000 0000 1100 110x	**Ch 7 Base / Current Address**	**RW**
0000 0000 1100 111x	**Ch 7 Base / Current Count**	**RW**
0000 0000 1101 000x	**Status / Command**	**RW**
0000 0000 1101 001x	**Write Request**	**WO**
0000 0000 1101 010x	**Write Single Mask**	**WO**
0000 0000 1101 011x	**Write Mode**	**WO**
0000 0000 1101 100x	**Clear Byte Pointer F/F**	**WO**
0000 0000 1101 101x	**Master Clear**	**WO**
0000 0000 1101 110x	**Clear Mask**	**WO**
0000 0000 1101 111x	**Read/Write All Mask Bits**	**WO**

Note that not all bits of the address are decoded.

The Master and Slave DMA Controllers are compatible with the Intel 8237 DMA Controller chip. Detailed description of 8237 DMA controller operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Ports 80-8F - DMA Page Registers

There are eight DMA Page Registers, one for each DMA channel. These registers provide bits 16-23 of the 24-bit address for each DMA channel (bits 0-15 are stored in registers in the Master and Slave DMA Controllers). They are located at the following I/O Port addresses:

I/O Address Bits 15-0	Register Name	
0000 0000 1000 0111	**Channel 0 DMA Page (M-0)**	**RW**
0000 0000 1000 0011	**Channel 1 DMA Page (M-1)**	**RW**
0000 0000 1000 0001	**Channel 2 DMA Page (M-2)**	**RW**
0000 0000 1000 0010	**Channel 3 DMA Page (M-3)**	**RW**
0000 0000 1000 1111	**Channel 4 DMA Page (S-0)**	**RW**
0000 0000 1000 1011	**Channel 5 DMA Page (S-1)**	**RW**
0000 0000 1000 1001	**Channel 6 DMA Page (S-2)**	**RW**
0000 0000 1000 1010	**Channel 7 DMA Page (S-3)**	**RW**

DMA Controller Shadow Registers

The DMA Controller shadow registers are enabled by setting function 0 Rx77 bit 0. If the shadow registers are enabled, they are read back at the indicated I/O port instead of the standard DMA controller registers (writes are unchanged).

Port 0 –Channel 0 Base Address .... RO
Port 1 –Channel 0 Byte Count .... RO
Port 2 –Channel 1 Base Address .... RO
Port 3 –Channel 1 Byte Count .... RO
Port 4 –Channel 2 Base Address .... RO
Port 5 –Channel 2 Byte Count .... RO
Port 6 –Channel 3 Base Address .... RO
Port 7 –Channel 3 Byte Count .... RO

Port 8 –1st Read Channel 0-3 Command Register .... RO
Port 8 –2nd Read Channel 0-3 Request Register .... RO
Port 8 –3rd Read Channel 0 Mode Register .... RO
Port 8 –4th Read Channel 1 Mode Register .... RO
Port 8 –5th Read Channel 2 Mode Register .... RO
Port 8 –6th Read Channel 3 Mode Register .... RO

Port F –Channel 0-3 Read All Mask .... RO

Port C4 –Channel 5 Base Address .... RO
Port C6 –Channel 5 Byte Count .... RO
Port C8 –Channel 6 Base Address .... RO
Port CA –Channel 6 Byte Count .... RO
Port CC –Channel 7 Base Address .... RO
Port CE –Channel 7 Byte Count .... RO

Port D0 –1st Read Channel 4-7 Command Register .... RO
Port D0 –2nd Read Channel 4-7 Request Register .... RO
Port D0 –3rd Read Channel 4 Mode Register .... RO
Port D0 –4th Read Channel 5 Mode Register .... RO
Port D0 –5th Read Channel 6 Mode Register .... RO
Port D0 –6th Read Channel 7 Mode Register .... RO

Port DE –Channel 4-7 Read All Mask .... RO

Interrupt Controller I/O Registers

Ports 20-21 - Master Interrupt Controller

The Master Interrupt Controller controls system interrupt channels 0-7. Two registers control the Master Interrupt Controller. They are:

I/O Address Bits 15-0	Register Name	
0000 0000 001x xxx0	**Master Interrupt Control**	**RW**
0000 0000 001x xxx1	**Master Interrupt Mask**	**RW**

Note that not all bits of the address are decoded.

The Master Interrupt Controller is compatible with the Intel 8259 Interrupt Controller chip. Detailed descriptions of 8259 Interrupt Controller operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Ports A0-A1 - Slave Interrupt Controller

The Slave Interrupt Controller controls system interrupt channels 8-15. The slave system interrupt controller also occupies two register locations:

I/O Address Bits 15-0	Register Name	
0000 0000 101x xxx0	**Slave Interrupt Control**	**RW**
0000 0000 101x xxx1	**Slave Interrupt Mask**	**RW**

Note that not all address bits are decoded.

The Slave Interrupt Controller is compatible with the Intel 8259 Interrupt Controller chip. Detailed descriptions of 8259 Interrupt Controller operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Interrupt Controller Shadow Registers

The following shadow registers are enabled by setting function 0 Rx47[4]. If the shadow registers are enabled, they are read back at the indicated I/O port instead of the standard interrupt controller registers (writes are unchanged).

Port 20 - Master Interrupt Control Shadow .... RO
Port A0 - Slave Interrupt Control Shadow...................... RO

7	**Reserved**	.... always reads 0
6	**OCW3 bit 2 (POLL)**	
5	**OCW3 bit 0 (RIS)**	
4	**OCW3 bit 5 (SMM)**	
3	**OCW2 bit 7 (R)**	
2	**ICW4 bit 4 (SFNM)**	
1	**ICW4 bit 1 (AEOI)**	
0	**ICW1 bit 3 (LTIM)**	

Port 21 - Master Interrupt Mask Shadow .... RO
Port A1 - Slave Interrupt Mask Shadow .... RO

7-5	**Reserved**	.... always reads 0
4-0	**T7-T3 of Interrupt Vector Address**	

Timer / Counter Registers

Ports 40-43 - Timer / Counter I/O Registers

There are 4 Timer / Counter registers:

I/O Address Bits 15-0	Register Name	
0000 0000 010x xx00	**Timer / Counter 0 Count**	**RW**
0000 0000 010x xx01	**Timer / Counter 1 Count**	**RW**
0000 0000 010x xx10	**Timer / Counter 2 Count**	**RW**
0000 0000 010x xx11	**Timer / Counter Cmd Mode**	**WO**

Note that not all bits of the address are decoded.

The Timer / Counters are compatible with the Intel 8254 Timer / Counter chip. Detailed descriptions of 8254 Timer / Counter operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Timer / Counter Shadow Registers

The following shadow registers are enabled for readback by setting function 0 Rx47[4]. If the shadow registers are enabled, they are read back at the indicated I/O port instead of the standard timer / counter registers (writes are unchanged).

Port 40 – Counter 0 Base Count Value (LSB 1st MSB 2nd)RO
Port 41 – Counter 1 Base Count Value (LSB 1st MSB 2nd)RO
Port 42 – Counter 2 Base Count Value (LSB 1st MSB 2nd)RO

CMOS / RTC I/O Registers

Port 70 - CMOS Address ....RW

7 NMI Disable.. RW
- 0 Enable NMI Generation. NMI is asserted on encountering SERR# on the PCI bus.
- 1 Disable NMI Generation .... default

6-0 CMOS Address (lower 128 bytes)....................... RW

Port 71 - CMOS Data..RW

7-0 CMOS Data (128 bytes)

Note: Ports 70-71 may be accessed if Device 17 Function 0 Rx51 bit-3 is set to one to select the internal RTC. If Rx51 bit-3 is set to zero, accesses to ports 70-71 will be directed to an external RTC.

Port 74 - CMOS Address ....RW

7-0 CMOS Address (256 bytes)................................ RW

Port 75 - CMOS Data..RW

7-0 CMOS Data (256 bytes)

Note: Ports 74-75 may be accessed only if Rx4E bit-3 (Port 74/75 Access Enable) is set to one to enable port 74/75 access.

Note: Ports 70-71 are compatible with PC industry-standards and may be used to access the lower 128 bytes of the 256-byte on-chip CMOS RAM. Ports 74-75 may be used to access the full on-chip extended 256-byte space in cases where the on-chip RTC is disabled.

Note: The system Real Time Clock (RTC) is part of the “CMOS” block. The RTC control registers are located at specific offsets in the CMOS data area (0-0Dh and 7D-7Fh). Detailed descriptions of CMOS / RTC operation and programming can be obtained from the VIA VT82887 Data Book or numerous other industry publications. For reference, the definition of the RTC register locations and bits are summarized in the following table:

Offset	Description		Binary Range	BCD Range
00	**Seconds**		00-3Bh	00-59h
01	**Seconds Alarm**		00-3Bh	00-59h
02	**Minutes**		00-3Bh	00-59h
03	**Minutes Alarm**		00-3Bh	00-59h
04	**Hours**	am 12hr:	01-1Ch	01-12h
		pm 12hr:	81-8Ch	81-92h
		24hr:	00-17h	00-23h
05	**Hours Alarm**	am 12hr:	01-1Ch	01-12h
		pm 12hr:	81-8Ch	81-92h
		24hr:	00-17h	00-23h
06	**Day of the Week**	Sun=1:	01-07h	01-07h
07	**Day of the Month**		01-1Fh	01-31h
08	**Month**		01-0Ch	01-12h
09	**Year**		00-63h	00-99h

0A Register A

Bit	Name	Description
7	**UIP**	Update In Progress
6-4	**DV2-0**	Divide (010=ena osc & keep time)
3-0	**RS3-0**	Rate Select for Periodic Interrupt

0B Register B

Bit	Name	Description
7	**SET**	Inhibit Update Transfers
6	**PIE**	Periodic Interrupt Enable
5	**AIE**	Alarm Interrupt Enable
4	**UIE**	Update Ended Interrupt Enable
3	**SQWE**	No function (read/write bit)
2	**DM**	Data Mode (0=BCD, 1=binary)
1	**24/12**	Hours Byte Format (0=12, 1=24)
0	**DSE**	Daylight Savings Enable

0C Register C

Bit	Name	Description
7	**IRQF**	Interrupt Request Flag
6	**PF**	Periodic Interrupt Flag
5	**AF**	Alarm Interrupt Flag
4	**UF**	Update Ended Flag
3-0	**0**	Unused (always read 0)

0D Register D

Bit	Name	Description
7	**VRT**	Reads 1 if VBAT voltage is OK
6-0	**0**	Unused (always read 0)

0E-7C Software-Defined Storage Registers (111 Bytes)

Offset	Extended Functions	Binary Range	BCD Range
7D	**Date Alarm**	01-1Fh	01-31h
7E	**Month Alarm**	01-0Ch	01-12h
7F	**Century Field**	13-14h	19-20h

80-FF Software-Defined Storage Registers (128 Bytes)

Table 9. CMOS Register Summary

Keyboard / Mouse Wakeup Index / Data Registers

The Keyboard / Mouse Wakeup registers are accessed by performing I/O operations to / from an index / data pair of registers in system I/O space at port addresses 2Eh and 2Fh. The registers accessed using this mechanism are used to initialize Keyboard / Mouse Wakeup functions at index values in the range of E0-EF.

Keyboard / Mouse Wakeup initialization is accomplished in three steps:

1) Enter initialization mode (set Function 0 Rx51[1] = 1)
2) Initialize the chip
   a) Write index to port 2Eh
   b) Read / write data from / to port 2Fh
   c) Repeat a and b for all desired registers
3) Exit initialization mode (set Function 0 Rx51[1] = 0)

Port 2Eh – Keyboard Wakeup Index ....RW

7-0 Index Value

Function 0 PCI configuration space register Rx51[1] must be set to 1 to enable access to the configuration registers.

Port 2Fh – Keyboard Wakeup Data ....RW

7-0 Data Value

Keyboard / Mouse Wakeup Registers

These registers are accessed via the port 2E / 2F index / data register pair with Function 0 Rx51[1] = 1 using the indicated index values below

Index E0 – Keyboard / Mouse Wakeup Enable (08h) ....RW

7-5 Reserved .... always reads 0

4 Reserved (Do Not Program).................... default = 0

3 Win98 Keyboard Power Key Wake-up
- 0 Disable
- 1 Enable**..default**

2 Password Wake-up
- 0 Disable .... default
- 1 Enable

1 PS/2 Mouse Wake-up
- 0 Disable .... default
- 1 Enable

0 Keyboard Wake-up
- 0 Disable .... default
- 1 Enable

Index E1 – Keyboard Wakeup Scan Code Set 0 (F0h).. RW

7-0 Keyboard Wakeup First Scan Code ....def = F0h

Index E2 – Keyboard Wakeup Scan Code Set 1 (00h) .. RW

7-0 Keyboard Wakeup Second Scan Code .....def = 00h

Index E3 – Keyboard Wakeup Scan Code Set 2 (00h) .. RW

7-0 Keyboard Wakeup Third Scan Code........def = 00h

Index E4 – Keyboard Wakeup Scan Code Set 3 (00h) .. RW

7-0 Keyboard Wakeup Fourth Scan Code......def = 00h

Index E5 – Keyboard Wakeup Scan Code Set 4 (00h) .. RW

7-0 Keyboard Wakeup Fifth Scan Code ....def = 00h

Index E6 – Keyboard Wakeup Scan Code Set 5 (00h) .. RW

7-0 Keyboard Wakeup Sixth Scan Code.........def = 00h

Index E7 – Keyboard Wakeup Scan Code Set 6 (00h) .. RW

7-0 Keyboard Wakeup Seventh Scan Code ....def = 00h

Index E8 – Keyboard Wakeup Scan Code Set 7 (00h) .. RW

7-0 Keyboard Wakeup Eighth Scan Code ......def = 00h

Index E9 –Mouse Wakeup Scan Code Set 1 (09h) .... RW

7-0 Mouse Wakeup Scan Code Set 1 ....def = 09h

Index EA –Mouse Wakeup Scan Code Set 2(00h) .... RW

7-0 Mouse Wakeup Scan Code Set 2 ....def = 00h

Index EB –Mouse Wakeup Scan Code Mask (00h) .... RW

7-0 Mouse Wakeup Scan Code Mask.............def = 00h

Memory Mapped I/O APIC Registers

Memory Address FEC00000 – APIC Index ....RW

7-0 APIC Index .... default = 00h
8-bit pointer to APIC registers.

Memory Address FEC00013-10 – APIC Data ....RW

31-0 APIC Data .... default = 0000 0000h
Data for the APIC register pointed to by the APIC index

Memory Address FEC00020 – APIC IRQ Pin AssertionWO

7-5 Reserved .... always reads 0
4-0 APIC IRQ Number ....default undefined
IRQ # for this interrupt. Valid values are 0-23 only.

Memory Address FEC00040 – APIC EOI .... WO

7-0 Redirection Entry Clear ....default undefined
When a write is issued to this register, the APIC will check this field and compare it with the vector field for each entry in the I/O redirection table. When a match is found, the "Remote_IRR" bit for that I/O Redirection Entry will be cleared.

Indexed I/O APIC Registers

Offset 0 – APIC Identification (0000 0000h) .... RW

31-28 Reserved ....always reads 0
27-24 APIC Identification ....default = 0
Software must program this value before using the APIC.
23-0 Reserved ....always reads 0

Offset 1 – APIC Version (00178003) .... RO

31-24 Reserved ....always reads 00h
23-16 Maximum Redirection ....always reads 17h
Equal to the number of APIC interrupt pins minus one. For this APIC, this value is 17h (23 decimal).
15 PCI IRQ
Always reads 1 to indicate that the IRQ assertion register is implemented and that PCI devices are allowed to write to it to cause interrupts.
14-8 Reserved ....always reads 0
7-0 APIC Version.................................always reads 03h
The implementation version for this APIC is 03h.

Offset 2 – APIC Arbitration (0000 0000h)....................... RO

31-28 Reserved ....always reads 00h
27-24 APIC Arbitration ID ....always reads 00h
23-0 Reserved ....always reads 00h

Offset 3 – Boot Configuration (0000 0000h) .... RW

31-1 Reserved ....always reads 00h
0 Interrupt Delivery Mechanism
- 0 APIC Serial Bus.................................... default
- 1 Front Side Bus Message

Offset 3F-10 – I/O Redirection Table

This table contains 24 registers, with one dedicated table entry for each of the 24 APIC interrupt signals. Each 64-bit register consists of two 32-bit values at consecutive index locations, with the low 32 bits at the even index and the upper 32 bits at the odd index. The default value for all registers is xxx1 xxxx xxxx xxxxh.

Offset 11-10 – I/O Redirection – APIC IRQ0 ....RW
Offset 13-12 – I/O Redirection – APIC IRQ1 ....RW
Offset 15-14 – I/O Redirection – APIC IRQ2 ....RW
Offset 17-16 – I/O Redirection – APIC IRQ3 ....RW
Offset 19-18 – I/O Redirection – APIC IRQ4 ....RW
Offset 1B-1A – I/O Redirection – APIC IRQ5................RW
Offset 1D-1C – I/O Redirection – APIC IRQ6................RW
Offset 1F-1E – I/O Redirection – APIC IRQ7 ....RW
Offset 21-20 – I/O Redirection – APIC IRQ8 ....RW
Offset 23-22 – I/O Redirection – APIC IRQ9 ....RW
Offset 25-24 – I/O Redirection – APIC IRQ10 ....RW
Offset 27-26 – I/O Redirection – APIC IRQ11 ....RW
Offset 29-28 – I/O Redirection – APIC IRQ12 ....RW
Offset 2B-2A – I/O Redirection – APIC IRQ13..............RW
Offset 2D-2C – I/O Redirection – APIC IRQ14..............RW
Offset 2F-2E – I/O Redirection – APIC IRQ15 ....RW
Offset 31-30 – I/O Redirection – APIC IRQ16 ....RW
Offset 33-32 – I/O Redirection – APIC IRQ17 ....RW
Offset 35-34 – I/O Redirection – APIC IRQ18 ....RW
Offset 37-36 – I/O Redirection – APIC IRQ19 ....RW
Offset 39-38 – I/O Redirection – APIC IRQ20 ....RW
Offset 3B-3A – I/O Redirection – APIC IRQ21..............RW
Offset 3D-3C – I/O Redirection – APIC IRQ22..............RW
Offset 3F-3E – I/O Redirection – APIC IRQ23 ....RW

Format for Each I/O Redirection Table Entry:

Physical Mode (bit-11=0)

63-60 Reserved .... always reads 0
59-56 APIC ID .... default = undefined

Logical Mode (bit-11=1)

63-56 Destination .... default = undefined

55-17 Reserved .... always reads 0

16 Interrupt Masked
- 0 Not masked .... default
- 1 Masked

15 Trigger Mode
- 0 Edge Sensitive .... default
- 1 Level Sensitive

14 Remote IRR (Level Sensitive Interrupts Only). RO
- 0 EOI message with a matching interrupt vector received from a local APIC
- 1 Level sensitive interrupt sent by IOAPIC accepted by local APIC(s)

13 Interrupt Input Pin Polarity
- 0 Active High... default
- 1 Active Low

12 Delivery Status... RO
Contains the current status of the delivery of this interrupt.
- 0 Idle (no activity)
- 1 Send Pending (the interrupt has been injected but its delivery is temporarily delayed either because the APIC bus is busy or because the receiving APIC unit cannot currently accept the interrupt)

11 Destination Mode
Determines the interpretation of bits 56-63.
- 0 Physical Mode .... default
- 1 Logical Mode

10-8 Delivery Mode
Specifies how the APICs listed in the destination field should act upon reception of this signal
- 000 Fixed .... default
- 001 Lowest Priority
- 010 SMI
- 011 -reserved-
- 100 NMI
- 101 INIT
- 110 -reserved-
- 111 External INT

7-0 Interrupt Vector
Contains the interrupt vector for this interrupt. Vector values range from 10h to FEh.

Configuration Space I/O

Configuration space accesses for all functions use PCI configuration mechanism 1 (see PCI specification revision 2.2 for more details). The ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

There are 8 "functions" implemented in the VT8235 (see Table 5 on page 21). The following sections describe the registers and register bits of these functions.

Port CFB-CF8 - Configuration Address ....RW

31 Configuration Space Enable
- 0 Disabled.. default
- 1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 Reserved .... always reads 0

23-16 PCI Bus Number
Used to choose a specific PCI bus in the system

15-11 Device Number
Used to choose a specific device in the system

10-8 Function Number
Used to choose a specific function if the selected device supports multiple functions

7-2 Register Number
Used to select a specific doubleword in the device's configuration space

1-0 Fixed .... always reads 0

Port CFF-CFC - Configuration Data ....RW

Device 16 Function 0 Registers - USB 1.1 UHCI Ports 0-1

This Universal Serial Bus host controller interface is fully compatible with UHCI specification v1.1. There are two sets of software accessible registers: PCI configuration registers and USB I/O registers. The PCI configuration registers are located in the Device 16 Function 0 PCI configuration space of the VT8235. The USB I/O registers are defined in UHCI specification v1.1. The registers in this function control USB ports 0-1 (see function 1 for ports 2-3 and function 2 for ports 4-5).

PCI Configuration Space Header

Offset 1-0 - Vendor ID (1106h).. RO

7-0 Vendor ID .... (1106h = VIA Technologies)

Offset 3-2 - Device ID (3038h) .... RO

7-0 Device ID .... (3038h = VT8235 USB Controller)

Offset 5-4 - Command (0000h) ....RW

15-8 Reserved .... always reads 0
7 Reserved (address stepping)........................ fixed at 0
6 Reserved (parity error response) .... fixed at 0
5 Reserved (VGA palette snoop) .... fixed at 0
4 Memory Write and Invalidate . default=0 (disabled)
3 Reserved (special cycle monitoring)........... fixed at 0
2 Bus Master .... default=0 (disabled)
1 Memory Space.......................... default=0 (disabled)
0 I/O Space .... default=0 (disabled)

Offset 7-6 - Status (0210h) ....RWC

15 Reserved (detected parity error).......... always reads 0
14 Signalled System Error............................. default=0
13 Received Master Abort.............................. default=0
12 Received Target Abort............................... default=0
11 Signalled Target Abort .... default=0
10-9 DEVSEL# Timing
00 Fast
01 Medium ....default (fixed)
10 Slow
11 Reserved
8-0 Reserved .... fixed 10h (PCI PMI)

Offset 8 - Revision ID (nnh) .... RO

7-0 Silicon Revision Code (0 indicates first silicon)

Offset 9 - Programming Interface (00h) .... RO

Offset A - Sub Class Code (03h=USB Controller) .... RO

Offset B - Base Class Code (0Ch=Serial Bus Controller)RO

Offset D - Latency Timer (16h) .... RW

Offset 23-20 - USB I/O Register Base Address............... RW

31-16 Reserved ....always reads 0
15-5 USB I/O Register Base Address. Port Address for the base of the 32-byte USB I/O Register block, corresponding to AD[15:5]
4-0 00001b

Offset 2D-2C - Sub Vendor ID (1106h)......................... RO†

Offset 2F-2E - Sub Device ID (3038h)........................... RO†

† RW if Rx42[4] = 1.

Offset 34 - Power Management Capabilities (80h) .... RW

Offset 3C - Interrupt Line (00h)...................................... RW

7-4 Reserved ....always reads 0
3-0 USB Interrupt Routing
0000 Disabled .... default
0001 IRQ1
0010 Reserved
0011 IRQ3
0100 IRQ4
0101 IRQ5
0110 IRQ6
0111 IRQ7
1000 IRQ8
1001 IRQ9
1010 IRQ10
1011 IRQ11
1100 IRQ12
1101 IRQ13
1110 IRQ14
1111 Disabled

Offset 3D - Interrupt Pin (01h)... RO

7-0 Interrupt Pin.........................default = 01h (INTA#)

USB-Specific Configuration Registers

Offset 40 - Miscellaneous Control 1 (40h) ....RW

- **7 Reserved** .... always reads 0
- **6 Babble Option**
  This bit controls whether the port is disabled when EOF (End-Of-Frame) babble occurs. Babble is unexpected bus activity that persists into the EOF interval. When this bit is 0, the port with the EOF babble is disabled. When it is 1, it is not disabled
  - 0 Automatically disable babbled port when EOF babble occurs
  - 1 Don't disable babbled port **...................default**
- **5 PCI Parity Check**
  - 0 Disable .... default
  - 1 Enable
- **4 Frame Interval Select**
  - 0 1 msec frame time .... default
  - 1 0.1 msec frame time
- **3 USB Data Length Option**
  - 0 Support TD length up to 1280............... default
  - 1 Support TD length up to 1023

  (TD = Transfer Descriptor)
- **2 Improve FIFO Latency**
  - 0 Improve latency if packet size < 64 bytes ... def
  - 1 Disable improvement
- **1 DMA Option**
  - 0 Enhanced performance (8 DW burst access with better FIFO latency) .... default
  - 1 Normal performance (16 DW burst access with normal FIFO latency)
- **0 Reserved** .... always reads 0

Offset 41 - Miscellaneous Control 2 (10h)...................... RW

- **7 USB 1.1 Improvement for EOP**
  This bit controls whether USB Specification 1.1 or 1.0 is followed when a stuffing error occurs before an EOP (End-Of-Packet). A stuffing error results when the receiver sees seven consecutive ones in a packet. Under USB specification 1.1, when this occurs in the interval just before an EOP, the receiver will accept the packet. Under USB specification 1.0, the packet is ignored.
  - 0 USB Spec 1.1 Compliant (packet accepted) def
  - 1 USB Spec 1.0 Compliant (packet ignored)
- **6-3 Reserved (Do Not Program)** ....default = 0
- **2 Trap Option**
  Under the UHCI spec, port 60 / 64 is trapped only when its corresponding enable bits are set. When this bit is set, trap can be set without checking the enable bits.
  - 0 Set trap 60/64 status bits only when trap 60/64 enable bits are set.................................. default
  - 1 Set trap 60/64 status bits without checking enable bits
- **1 A20Gate Pass Through Option**
  This bit controls whether the A20Gate pass-through sequence (as defined in UHCI) is followed. The A20Gate sequence consists of 4 commands. When this bit is 0, the 4-command sequence is followed. When this bit is 1, the last command (write FFh to port 64) is skipped.
  - 0 A20GATE Pass-through command sequence as defined in UHCI .... default
  - 1 Last command skipped
- **0 Reserved (Do Not Program)** ....default = 0

Offset 42 - Miscellaneous Control 3 (03h) .... RW

7 **Reserved (Do Not Program)** .... default = 0
6-5 **Reserved** .... always reads 0
4 **SubVendor ID / SubDevice ID Backdoor**
- 0 Rx2C-2F RO .... default
- 1 Rx2C-2F RW

3-2 **Reserved (Do Not Program)** .... default = 0
1-0 **Reserved** **................................. always reads 11b**

Offset 43 - Miscellaneous Control 4 (00h) .... RW

7-5 **Reserved** .... always reads 0
4 **Reserved (Do Not Program)** .... default = 0
3 **Continue Transmission of Erroneous Data on FIFO Underrun**
- 0 Enable.. default
- 1 Disable

2 **Issue CRC Error Instead of Stuffing Error on FIFO Underrun**
- 0 Enable.. default
- 1 Disable

1-0 **Reserved** .... always reads 0

Offset 48 - Miscellaneous Control 5 .... RW

7-5 **Reserved** .... always reads 0
4-3 **Reserved (Do Not Program)** .... default = 0
2 **Issue Bad CRC5 in SOF After FIFO Underrun**
- 0 Enable.. default
- 1 Disable

1 **Lengthen PreSOF Time**
The preSOF time point determines whether there is enough timein the remaining frame period to perform a 64-byte transaction. It prevents a packet that may not fit in the remaining frame period from being initiated. This bit controls whether the preSOF time point is moved back so that the preSOF time is lengthened.
- 0 Disable .... default
- 1 Enable (PreSOF time lengthened)

0 **Issue Nonzero Bad CRC Code on FIFO Underrun**
A FIFO underrun occurs when there is no data in the FIFO to supply data transmission. When this occurs, the south bridge invalidates the data by sending an incorrect CRC code to the device. This bit controls the type of incorrect CRC sent.
- 0 Non zero CRC (recommended)............. default
- 1 All zero CRC

This option isn't really needed any more as non-zero CRC always works.

Offset 49 - Miscellaneous Control 6 (03h)....................... RW

7-6 **Reserved** .... always reads 0
5-4 **Reserved (Do Not Program)** .... default = 0
3-2 **Reserved** .... always reads 0
1 **EHCI Supports PME Assertion in D3 Cold State**
- 0 Not Supported
- 1 Supported... **default**

0 **UHCI Supports PME Assertion in D3 Cold State**
- 0 Not Supported
- 1 Supported... **default**

Offset 4A - Miscellaneous Control 7 (00h)...................... RW

7-3 **Reserved** .... always reads 0
2 **Reserved (Do Not Program)** .... default = 0
1 **Reserved** .... always reads 0
0 **Use External 60 MHz Clock**
- 0 Disable .... default
- 1 Enable

Offset 60 - Serial Bus Release Number .... RO

7-0 **Release Number** .... always reads 10h

Offset 84 – PM Capability Status .... RW

7-0 **PM Capability Status**
- 00 D0 .... default
- 01 -reserved-
- 10 -reserved-
- 11 D3 Hot

Offset C1-C0 - Legacy Support .... RO

15-0 **UHCI v1.1 Compliant** .... always reads 2000h

USB I/O Registers

These registers are compliant with the UHCI v1.1 standard. Refer to the UHCI v1.1 specification for further details.

I/O Offset 1-0 - USB Command

I/O Offset 3-2 - USB Status

I/O Offset 5-4 - USB Interrupt Enable

I/O Offset 7-6 - Frame Number

I/O Offset B-8 - Frame List Base Address

I/O Offset 0C - Start Of Frame Modify

I/O Offset 11-10 - Port 0 Status / Control

I/O Offset 13-12 - Port 1 Status / Control

Device 16 Function 1 Registers - USB 1.1 UHCI Ports 2-3

This Universal Serial Bus host controller interface is fully compatible with UHCI specification v1.1. There are two sets of software accessible registers: PCI configuration registers and USB I/O registers. The PCI configuration registers are located in the Device 16 Function 1 PCI configuration space of the VT8235. The USB I/O registers are defined in UHCI specification v1.1. The registers in this function control USB ports 2-3 (see function 0 for ports 0-1 and function 2 for ports 4-5).

PCI Configuration Space Header

Offset 1-0 - Vendor ID (1106h).. RO

7-0	**Vendor ID**	.... (1106h = VIA Technologies)

Offset 3-2 - Device ID (3038h) .... RO

7-0	**Device ID**	.... (3038h = VT8235 USB Controller)

Offset 5-4 - Command (0000h) ....RW

15-8	**Reserved**	.... always reads 0
7	**Reserved** (address stepping)	.... fixed at 0
6	**Reserved** (parity error response)	.... fixed at 0
5	**Reserved** (VGA palette snoop)	.... fixed at 0
4	**Memory Write and Invalidate**	. default=0 (disabled)
3	**Reserved** (special cycle monitoring)	.... fixed at 0
2	**Bus Master**	.... default=0 (disabled)
1	**Memory Space**	.... default=0 (disabled)
0	**I/O Space**	.... default=0 (disabled)

Offset 7-6 - Status (0210h) ....RWC

15	**Reserved** (detected parity error)	.... always reads 0
14	**Signalled System Error**	.... default=0
13	**Received Master Abort**	.... default=0
12	**Received Target Abort**	.... default=0
11	**Signalled Target Abort**	.... default=0
10-9	**DEVSEL# Timing**	
	00 Fast	
	01 Medium	.....................................default (fixed)
	10 Slow	
	11 Reserved	
8-0	**Reserved**	.... fixed 10h (PCI PMI)

Offset 8 - Revision ID (nnh) .... RO

7-0	Silicon Revision Code (0 indicates first silicon)

Offset 9 - Programming Interface (00h) .... RO

Offset A - Sub Class Code (03h=USB Controller) .... RO

Offset B - Base Class Code (0Ch=Serial Bus Controller)RO

Offset D - Latency Timer (16h) .... RW

Offset 23-20 - USB I/O Register Base Address............... RW

31-16	**Reserved**	....always reads 0
15-5	**USB I/O Register Base Address.** Port Address for the base of the 32-byte USB I/O Register block, corresponding to AD[15:5]	
4-0	**00001b**	

Offset 2D-2C - Sub Vendor ID (1106h).......................... RO†

Offset 2F-2E - Sub Device ID (3038h)............................ RO†

† RW if Rx42[4] = 1.

Offset 34 - Power Management Capabilities (80h) .... RW

Offset 3C - Interrupt Line (00h)...................................... RW

7-4	**Reserved**	....always reads 0
3-0	**USB Interrupt Routing**	
	0000 Disabled	.... default
	0001 IRQ1	
	0010 Reserved	
	0011 IRQ3	
	0100 IRQ4	
	0101 IRQ5	
	0110 IRQ6	
	0111 IRQ7	
	1000 IRQ8	
	1001 IRQ9	
	1010 IRQ10	
	1011 IRQ11	
	1100 IRQ12	
	1101 IRQ13	
	1110 IRQ14	
	1111 Disabled	

Offset 3D - Interrupt Pin (02h)... RO

7-0	**Interrupt Pin**	.........................default = 02h (INTB#)

USB-Specific Configuration Registers

Offset 40 - Miscellaneous Control 1 (40h) .... RW

7 Reserved .... always reads 0

6 Babble Option

This bit controls whether the port is disabled when EOF (End-Of-Frame) babble occurs. Babble is unexpected bus activity that persists into the EOF interval. When this bit is 0, the port with the EOF babble is disabled. When it is 1, it is not disabled

- 0 Automatically disable babbled port when EOF babble occurs
- 1 Don't disable babbled port **.................... default**

5 PCI Parity Check

- 0 Disable .... default
- 1 Enable

4 Frame Interval Select

- 0 1 msec frame time .... default
- 1 0.1 msec frame time

3 USB Data Length Option

- 0 Support TD length up to 1280 .... default
- 1 Support TD length up to 1023

(TD = Transfer Descriptor)

2 Improve FIFO Latency

- 0 Improve latency if packet size < 64 bytes ... def
- 1 Disable improvement

1 DMA Option

- 0 Enhanced performance (8 DW burst access with better FIFO latency) .... default
- 1 Normal performance (16 DW burst access with normal FIFO latency)

0 Reserved .... always reads 0

Offset 41 - Miscellaneous Control 2 (10h) .... RW

7 USB 1.1 Improvement for EOP

This bit controls whether USB Specification 1.1 or 1.0 is followed when a stuffing error occurs before an EOP (End-Of-Packet). A stuffing error results when the receiver sees seven consecutive ones in a packet. Under USB specification 1.1, when this occurs in the interval just before an EOP, the receiver will accept the packet. Under USB specification 1.0, the packet is ignored.

- 0 USB Spec 1.1 Compliant (packet accepted) def
- 1 USB Spec 1.0 Compliant (packet ignored)

6-3 Reserved (Do Not Program) .... default = 0

2 Trap Option

Under the UHCI spec, port 60 / 64 is trapped only when its corresponding enable bits are set. When this bit is set, trap can be set without checking the enable bits.

- 0 Set trap 60/64 status bits only when trap 60/64 enable bits are set .... default
- 1 Set trap 60/64 status bits without checking enable bits

1 A20Gate Pass Through Option

This bit controls whether the A20Gate pass-through sequence (as defined in UHCI) is followed. The A20Gate sequence consists of 4 commands. When this bit is 0, the 4-command sequence is followed. When this bit is 1, the last command (write FFh to port 64) is skipped.

- 0 A20GATE Pass-through command sequence as defined in UHCI .... default
- 1 Last command skipped

0 Reserved (Do Not Program) .... default = 0

Offset 42 - Miscellaneous Control 3 (03h) ....RW

- **7 Reserved (Do Not Program)** .... default = 0
- **6-5 Reserved** .... always reads 0
- **4 SubVendor ID / SubDevice ID Backdoor**
  - 0 Rx2C-2F RO .... default
  - 1 Rx2C-2F RW
- **3-2 Reserved (Do Not Program)** .... default = 0
- **1-0 Reserved** .... **always reads 11b**

Offset 43 - Miscellaneous Control 4 (00h) ....RW

- **7-5 Reserved** .... always reads 0
- **4 Reserved (Do Not Program)** .... default = 0
- **3 Continue Transmission of Erroneous Data on FIFO Underrun**
  - 0 Enable.. default
  - 1 Disable
- **2 Issue CRC Error Instead of Stuffing Error on FIFO Underrun**
  - 0 Enable.. default
  - 1 Disable
- **1-0 Reserved** .... always reads 0

Offset 48 - Miscellaneous Control 5 ....RW

- **7-5 Reserved** .... always reads 0
- **4-3 Reserved (Do Not Program)** .... default = 0
- **2 Issue Bad CRC5 in SOF After FIFO Underrun**
  - 0 Enable.. default
  - 1 Disable
- **1 Lengthen PreSOF Time**
  The preSOF time point determines whether there is enough timein the remaining frame period to perform a 64-byte transaction. It prevents a packet that may not fit in the remaining frame period from being initiated. This bit controls whether the preSOF time point is moved back so that the preSOF time is lengthened.
  - 0 Disable .... default
  - 1 Enable (PreSOF time lengthened)
- **0 Issue Nonzero Bad CRC Code on FIFO Underrun**
  A FIFO underrun occurs when there is no data in the FIFO to supply data transmission. When this occurs, the south bridge invalidates the data by sending an incorrect CRC code to the device. This bit controls the type of incorrect CRC sent.
  - 0 Non zero CRC (recommended)............ default
  - 1 All zero CRC

  This option isn't really needed any more as non-zero CRC always works.

Offset 49 - Miscellaneous Control 6 (03h)...................... RW

- **7-6 Reserved** ....always reads 0
- **5-4 Reserved (Do Not Program)** ....default = 0
- **3-2 Reserved** ....always reads 0
- **1 EHCI Supports PME Assertion in D3 Cold State**
  - 0 Not Supported
  - 1 Supported.. **default**
- **0 UHCI Supports PME Assertion in D3 Cold State**
  - 0 Not Supported
  - 1 Supported.. **default**

Offset 4A - Miscellaneous Control 7 (00h)..................... RW

- **7-3 Reserved** ....always reads 0
- **2 Reserved (Do Not Program)** ....default = 0
- **1 Reserved** ....always reads 0
- **0 Use External 60 MHz Clock**
  - 0 Disable ....default
  - 1 Enable

Offset 60 - Serial Bus Release Number .... RO

- **7-0 Release Number** ....always reads 10h

Offset 84 – PM Capability Status .... RW

- **7-0 PM Capability Status**
  - 00 D0 ....default
  - 01 -reserved-
  - 10 -reserved-
  - 11 D3 Hot

Offset C1-C0 - Legacy Support .... RO

- **15-0 UHCI v1.1 Compliant** ....always reads 2000h

USB I/O Registers

These registers are compliant with the UHCI v1.1 standard. Refer to the UHCI v1.1 specification for further details.

I/O Offset 1-0 - USB Command

I/O Offset 3-2 - USB Status

I/O Offset 5-4 - USB Interrupt Enable

I/O Offset 7-6 - Frame Number

I/O Offset B-8 - Frame List Base Address

I/O Offset 0C - Start Of Frame Modify

I/O Offset 11-10 - Port 0 Status / Control

I/O Offset 13-12 - Port 1 Status / Control

Device 16 Function 2 Registers - USB 1.1 UHCI Ports 4-5

This Universal Serial Bus host controller interface is fully compatible with UHCI specification v1.1. There are two sets of software accessible registers: PCI configuration registers and USB I/O registers. The PCI configuration registers are located in the Device 16 Function 0 PCI configuration space of the VT8235. The USB I/O registers are defined in UHCI specification v1.1. The registers in this function control USB ports 4-5 (see function 0 for ports 0-1 and function 1 for ports 2-3).

PCI Configuration Space Header

Offset 1-0 - Vendor ID (1106h).. RO

7-0 **Vendor ID** .... (1106h = VIA Technologies)

Offset 3-2 - Device ID (3038h) .... RO

7-0 **Device ID** .... (3038h = VT8235 USB Controller)

Offset 5-4 - Command (0000h) ....RW

15-8 **Reserved** .... always reads 0
7 **Reserved** (address stepping)........................ fixed at 0
6 **Reserved** (parity error response) .... fixed at 0
5 **Reserved** (VGA palette snoop) .... fixed at 0
4 **Memory Write and Invalidate** . default=0 (disabled)
3 **Reserved** (special cycle monitoring)........... fixed at 0
2 **Bus Master** .... default=0 (disabled)
1 **Memory Space**.......................... default=0 (disabled)
0 **I/O Space** .... default=0 (disabled)

Offset 7-6 - Status (0210h) ....RWC

15 **Reserved** (detected parity error).......... always reads 0
14 **Signalled System Error**............................. default=0
13 **Received Master Abort**............................. default=0
12 **Received Target Abort**.............................. default=0
11 **Signalled Target Abort** .... default=0
10-9 **DEVSEL# Timing**
  00 Fast
  01 Medium ....default (fixed)
  10 Slow
  11 Reserved
8-0 **Reserved** .... fixed 10h (PCI PMI)

Offset 8 - Revision ID (nnh) .... RO

7-0 Silicon Revision Code (0 indicates first silicon)

Offset 9 - Programming Interface (00h) .... RO

Offset A - Sub Class Code (03h=USB Controller) .... RO

Offset B - Base Class Code (0Ch=Serial Bus Controller)RO

Offset D - Latency Timer (16h) .... RW

Offset 23-20 - USB I/O Register Base Address............... RW

31-16 **Reserved** ....always reads 0
15-5 **USB I/O Register Base Address.** Port Address for the base of the 32-byte USB I/O Register block, corresponding to AD[15:5]
4-0 **00001b**

Offset 2D-2C - Sub Vendor ID (1106h).......................... RO†

Offset 2F-2E - Sub Device ID (3038h)............................ RO†

† RW if Rx42[4] = 1.

Offset 34 - Power Management Capabilities (80h) .... RW

Offset 3C - Interrupt Line (00h)...................................... RW

7-4 **Reserved** ....always reads 0
3-0 **USB Interrupt Routing**
  0000 Disabled .... default
  0001 IRQ1
  0010 Reserved
  0011 IRQ3
  0100 IRQ4
  0101 IRQ5
  0110 IRQ6
  0111 IRQ7
  1000 IRQ8
  1001 IRQ9
  1010 IRQ10
  1011 IRQ11
  1100 IRQ12
  1101 IRQ13
  1110 IRQ14
  1111 Disabled

Offset 3D - Interrupt Pin (03h).. RO

7-0 **Interrupt Pin** ....default = 03h (INTC#)

USB-Specific Configuration Registers

Offset 40 - Miscellaneous Control 1 (40h) ....RW

- **7 Reserved** .... always reads 0
- **6 Babble Option**
  This bit controls whether the port is disabled when EOF (End-Of-Frame) babble occurs. Babble is unexpected bus activity that persists into the EOF interval. When this bit is 0, the port with the EOF babble is disabled. When it is 1, it is not disabled
  - 0 Automatically disable babbled port when EOF babble occurs
  - 1 Don't disable babbled port **....................default**
- **5 PCI Parity Check**
  - 0 Disable .... default
  - 1 Enable
- **4 Frame Interval Select**
  - 0 1 msec frame time .... default
  - 1 0.1 msec frame time
- **3 USB Data Length Option**
  - 0 Support TD length up to 1280............... default
  - 1 Support TD length up to 1023

  (TD = Transfer Descriptor)
- **2 Improve FIFO Latency**
  - 0 Improve latency if packet size < 64 bytes ... def
  - 1 Disable improvement
- **1 DMA Option**
  - 0 Enhanced performance (8 DW burst access with better FIFO latency) .... default
  - 1 Normal performance (16 DW burst access with normal FIFO latency)
- **0 Reserved** .... always reads 0

Offset 41 - Miscellaneous Control 2 (10h)...................... RW

- **7 USB 1.1 Improvement for EOP**
  This bit controls whether USB Specification 1.1 or 1.0 is followed when a stuffing error occurs before an EOP (End-Of-Packet). A stuffing error results when the receiver sees seven consecutive ones in a packet. Under USB specification 1.1, when this occurs in the interval just before an EOP, the receiver will accept the packet. Under USB specification 1.0, the packet is ignored.
  - 0 USB Spec 1.1 Compliant (packet accepted) def
  - 1 USB Spec 1.0 Compliant (packet ignored)
- **6-3 Reserved (Do Not Program)** ....default = 0
- **2 Trap Option**
  Under the UHCI spec, port 60 / 64 is trapped only when its corresponding enable bits are set. When this bit is set, trap can be set without checking the enable bits.
  - 0 Set trap 60/64 status bits only when trap 60/64 enable bits are set.................................. default
  - 1 Set trap 60/64 status bits without checking enable bits
- **1 A20Gate Pass Through Option**
  This bit controls whether the A20Gate pass-through sequence (as defined in UHCI) is followed. The A20Gate sequence consists of 4 commands. When this bit is 0, the 4-command sequence is followed. When this bit is 1, the last command (write FFh to port 64) is skipped.
  - 0 A20GATE Pass-through command sequence as defined in UHCI .... default
  - 1 Last command skipped
- **0 Reserved (Do Not Program)** ....default = 0

Offset 42 - Miscellaneous Control 3 (03h) ....RW

- **7 Reserved (Do Not Program)** .... default = 0
- **6-5 Reserved** .... always reads 0
- **4 SubVendor ID / SubDevice ID Backdoor**
  - 0 Rx2C-2F RO .... default
  - 1 Rx2C-2F RW
- **3-2 Reserved (Do Not Program)** .... default = 0
- **1-0 Reserved .... always reads 11b**

Offset 43 - Miscellaneous Control 4 (00h) ....RW

- **7-5 Reserved** .... always reads 0
- **4 Reserved (Do Not Program)** .... default = 0
- **3 Continue Transmission of Erroneous Data on FIFO Underrun**
  - 0 Enable... default
  - 1 Disable
- **2 Issue CRC Error Instead of Stuffing Error on FIFO Underrun**
  - 0 Enable... default
  - 1 Disable
- **1-0 Reserved** .... always reads 0

Offset 48 - Miscellaneous Control 5 ....RW

- **7-5 Reserved** .... always reads 0
- **4-3 Reserved (Do Not Program)** .... default = 0
- **2 Issue Bad CRC5 in SOF After FIFO Underrun**
  - 0 Enable... default
  - 1 Disable
- **1 Lengthen PreSOF Time**
  The preSOF time point determines whether there is enough timein the remaining frame period to perform a 64-byte transaction. It prevents a packet that may not fit in the remaining frame period from being initiated. This bit controls whether the preSOF time point is moved back so that the preSOF time is lengthened.
  - 0 Disable .... default
  - 1 Enable (PreSOF time lengthened)
- **0 Issue Nonzero Bad CRC Code on FIFO Underrun**
  A FIFO underrun occurs when there is no data in the FIFO to supply data transmission. When this occurs, the south bridge invalidates the data by sending an incorrect CRC code to the device. This bit controls the type of incorrect CRC sent.
  - 0 Non zero CRC (recommended)............ default
  - 1 All zero CRC

  This option isn't really needed any more as non-zero CRC always works.

Offset 49 - Miscellaneous Control 6 (03h)...................... RW

- **7-6 Reserved** ....always reads 0
- **5-4 Reserved (Do Not Program)** ....default = 0
- **3-2 Reserved** ....always reads 0
- **1 EHCI Supports PME Assertion in D3 Cold State**
  - 0 Not Supported
  - 1 Supported**.. default**
- **0 UHCI Supports PME Assertion in D3 Cold State**
  - 0 Not Supported
  - 1 Supported**.. default**

Offset 4A - Miscellaneous Control 7 (00h)..................... RW

- **7-3 Reserved** ....always reads 0
- **2 Reserved (Do Not Program)** ....default = 0
- **1 Reserved** ....always reads 0
- **0 Use External 60 MHz Clock**
  - 0 Disable .... default
  - 1 Enable

Offset 60 - Serial Bus Release Number .... RO

- **7-0 Release Number**.............................always reads 10h

Offset 84 – PM Capability Status .... RW

- **7-0 PM Capability Status**
  - 00 D0 .... default
  - 01 -reserved-
  - 10 -reserved-
  - 11 D3 Hot

Offset C1-C0 - Legacy Support .... RO

- **15-0 UHCI v1.1 Compliant** ....always reads 2000h

USB I/O Registers

These registers are compliant with the UHCI v1.1 standard. Refer to the UHCI v1.1 specification for further details.

I/O Offset 1-0 - USB Command

I/O Offset 3-2 - USB Status

I/O Offset 5-4 - USB Interrupt Enable

I/O Offset 7-6 - Frame Number

I/O Offset B-8 - Frame List Base Address

I/O Offset 0C - Start Of Frame Modify

I/O Offset 11-10 - Port 0 Status / Control

I/O Offset 13-12 - Port 1 Status / Control

Device 16 Function 3 Registers - USB 2.0 EHCI

This Enhanced Serial Bus host controller interface is fully compatible with EHCI specification v1.0. There are two sets of software accessible registers: PCI configuration registers and USB I/O registers. The PCI configuration registers are located in the Device 16 Function 3 PCI configuration space of the VT8235. The USB I/O registers are defined in EHCI specification v1.0. The registers in this function control USB 2.0 functions (see functions 0-2 for USB 1.1 UHCI control).

PCI Configuration Space Header

Offset 1-0 - Vendor ID (1106h).. RO

7-0	**Vendor ID**	.... (1106h = VIA Technologies)

Offset 3-2 - Device ID (3104h)... RO

7-0	**Device ID**	(3104h = VT8235 USB 2.0 EHCI Controller)

Offset 5-4 - Command (0000h)...RW

15-8	**Reserved**	.... always reads 0
7	**Address Stepping**	.... default=0 (disabled)
6	**Reserved** (parity error response)	.... fixed at 0
5	**Reserved** (VGA palette snoop)	.... fixed at 0
4	**Memory Write and Invalidate**	. default=0 (disabled)
3	**Reserved** (special cycle monitoring)	.... fixed at 0
2	**Bus Master**	.... default=0 (disabled)
1	**Memory Space**	.... default=0 (disabled)
0	**I/O Space**	.... default=0 (disabled)

Offset 7-6 - Status (0210h) ....RWC

15	**Reserved** (detected parity error)	.... always reads 0
14	**Signaled System Error**	.... default=0
13	**Received Master Abort**	.... default=0
12	**Received Target Abort**	.... default=0
11	**Signaled Target Abort**	.... default=0
10-9	**DEVSEL# Timing**	00 Fast 01 Medium ....default (fixed) 10 Slow 11 Reserved
8-0	**Reserved**	.... fixed 10h (PCI PMI)

Offset 8 - Revision ID (nnh)... RO

7-0	Silicon Revision Code

Offset 9 - Programming Interface (20h) .... RO

Offset A - Sub Class Code (03h=USB Controller) .... RO

Offset B - Base Class Code (0Ch=Serial Bus Controller)RO

Offset C – Cache Line Size (10h)..................................... RW

Offset D - Latency Timer (16h) .... RW

Offset 13-10 – EHCI Memory Mapped I/O Base Addr. RW

31-8	**EHCI Memory Mapped I/O Registers Base Address.** Memory Address for the base of the USB 2.0 EHCI I/O Register block, corresponding to AD[31:8]	
7-3	**Reserved**	....always reads 0
2-1	**Memory Mapping**	.....reads 00b for 32-bit addressing
0	**Reserved**	....always reads 0

Offset 2D-2C - Sub Vendor ID (1106h)......................... RO†

Offset 2F-2E - Sub Device ID (3104h)........................... RO†

† RW if Rx42[4] = 1.

Offset 34 - Power Management Capabilities (80h) .... RW

Offset 3C - Interrupt Line (00h)...................................... RW

7-4	**Reserved**	....always reads 0
3-0	**USB Interrupt Routing**	0000 Disabled .... default 0001 IRQ1 0010 Reserved 0011 IRQ3 0100 IRQ4 0101 IRQ5 0110 IRQ6 0111 IRQ7 1000 IRQ8 1001 IRQ9 1010 IRQ10 1011 IRQ11 1100 IRQ12 1101 IRQ13 1110 IRQ14 1111 Disabled

Offset 3D - Interrupt Pin (04h).. RO

7-0	**Interrupt Pin**	.........................default = 04h (INTD#)

USB-Specific Configuration Registers

Offset 40 - Miscellaneous Control 1 (40h) ....RW

- **7 Reserved** .... always reads 0
- **6 Babble Option**
  This bit controls whether the port is disabled when EOF (End-Of-Frame) babble occurs. Babble is unexpected bus activity that persists into the EOF interval. When this bit is 0, the port with the EOF babble is disabled. When it is 1, it is not disabled
  - 0 Automatically disable babbled port when EOF babble occurs
  - 1 Don't disable babbled port ....**default**
- **5 PCI Parity Check**
  - 0 Disable .... default
  - 1 Enable
- **4 Reserved (Do Not Program)**.................... default = 0
- **3-2 Reserved** .... always reads 0
- **1 DMA Options**
  - 0 16 DW burst access .... default
  - 1 8 DW burst access
- **0 Reserved** .... always reads 0

Offset 48 - Miscellaneous Control 1 (A0h) ....RW

- **7-6 Reserved (Do Not Program)**.................... default = 0
- **5 CCA Burst Access**
  - 0 Burst enable
  - 1 Burst disable...**default**
- **4-1 Reserved** .... always reads 0
- **0 Reserved (Do Not Program)**.................... default = 0

Offset 49 - Miscellaneous Control 2 (20h) ....RW

- **7-6 Reserved (Do Not Program)**.................... default = 0
- **5 Clock Auto Stop**
  - 0 Disable, no stop
  - 1 Enable, auto stop ....**default**
- **4 Auto Power Down Receiver Squelch Detector**
  - 0 Auto Power Down................................. default
  - 1 Always Powered Up
- **3-0 Reserved** .... always reads 0

Offset 60 - Serial Bus Release Number (20h) .... RO

- **7-0 Release Number**..........always reads 20h for USB 2.0

Offset 61 - Frame Length Adjust (20h)........................... RO

Offset 63-62 – Port Wake Capability (0001h) .... RO

Offset 6B-68 - Legacy Support Extended Capability ..... RO

- **31-0 Capabilities** ....always reads 0000 0001h

Offset 6F-6C - Legacy Support Control / Status............ RW

- **31-0 Control / Status**..................always reads 0000 0000h

Offset 84 – PM Capability Status .... RW

- **7-0 PM Capability Status**
  - 00 D0 .... default
  - 01 -reserved-
  - 10 -reserved-
  - 11 D3 Hot

EHCI USB 2.0 I/O Registers

These registers are compliant with the EHCI v1.0 standard. Refer to the EHCI v1.0 specification for further details.

EHCI Capabilities

I/O Offset 0 - Capability Register Length (10h)

I/O Offset 3-2 - Interface Version Number (0100h) ......RO†
I/O Offset 7-4 – Structure Parameters (0000 3206h) ....RO†
I/O Offset B-8 – Capability Parameters (0000 6872h) .RO†
† RW if Rx42[4] = 1.

Host Controller Operations

I/O Offset 13-10 - USB Command

I/O Offset 17-14 - USB Status

I/O Offset 1B-18 - USB Interrupt Enable

I/O Offset 1F-1C - USB Frame Index

I/O Offset 23-20 - 4G Segment Selector

I/O Offset 27-24 - Frame List Base Address

I/O Offset 2B-28 - Next Asynchronous List Address

I/O Offset 53-50 - Configured Flags

I/O Offset 57-54 - Port 0 Status / Control

I/O Offset 5B-58 - Port 1 Status / Control

Device 17 Function 0 Registers – Bus Control and Power Management

All registers are located in the device 17 function 0 configuration space of the VT8235. These registers are accessed through PCI configuration mechanism #1 via I/O address 0CF8h / 0CFCh.

PCI Configuration Space Header

Offset 1-0 - Vendor ID (1106h).. RO

Offset 3-2 - Device ID (3177h) .... RO

Offset 5-4 - Command...RW

15-8	**Reserved**	.... always reads 0
7	**Address / Data Stepping**	
	0 Disable	
	1 Enable	.... default
6-4	**Reserved**	.... always reads 0
3	**Special Cycle Enable**	........................RW, default = 0
2	**Bus Master**	.... always reads 1
1	**Memory Space**	.... RO, reads as 1
0	**I/O Space**	.... RO, reads as 1

Offset 7-6 - Status...RWC

15	**Detected Parity Error**	....................write one to clear
14	**Signalled System Error**	.... always reads 0
13	**Signalled Master Abort**	.................write one to clear
12	**Received Target Abort**	...................write one to clear
11	**Signalled Target Abort**	..................write one to clear
10-9	**DEVSEL# Timing**	....................fixed at 01 (medium)
8	**Data Parity Detected** Reads 1 if PERR# is asserted (driven or observed) or a bus master data parity error occurred.	
7	**Fast Back-to-Back Capable**	.... always reads 0
6-0	**Reserved**	.... always reads 0

Offset 8 - Revision ID (nnh) ....RO

7-0	**Revision ID**

Offset 9 - Program Interface (00h)...................................RO

Offset A - Sub Class Code (01h) ....RO

Offset B - Class Code (06h)...RO

Offset E - Header Type (80h)..RO

7-0	**Header Type Code.........** 80h (Multifunction Device)

Offset F - BIST (00h)...RO

Offset 2F-2C - Subsystem ID ....RO

Use offset 70-73 to change the value returned.

ISA Bus Control

Offset 40 - ISA Bus Control (00h) .... RW

- **7 ISA Command Delay**
  - 0 Normal .... default
  - 1 Extra
- **6 I/O Recovery Time**
  The number of clocks between 2 I/O commands
  - 0 Disable .... default
  - 1 Enable (Rx4C[7:6] determines the # of clocks)
- **5 ROM Wait States**
  - 0 1 Wait State .... default
  - 1 0 Wait States
- **4 ROM Write**
  - 0 Disable (ROM writes are ignored) .... default
  - 1 Enable (ROM can be written)
- **3 Double DMA Clock**
  - 0 DMA clock runs at 4 MHz .... default
  - 1 DMA clock runs at 8 MHz
- **2 4D0 / 4D1 Port Configuration**
  Controls whether ports 4D0 / 4D1 can be configured. Ports 4D0 / 4D1 determine whether IRQ requests are edge or level triggerred (4D0[7-0] for IRQ7-0, 4D1[7-0] for IRQ15-8) (0 = level, 1 = edge).
  - 0 Disable .... default
  - 1 Enable
- **1 DMA / Interrupt / Timer Shadow Register Read**
  - 0 Disable .... default
  - 1 Enable (shadow register values can be read)
- **0 Double ISA Bus Clock**
  - 0 Bus clock runs at PCLK / 4 (8 MHz) .... default
  - 1 Bus clock runs at PCLK / 2 (16 MHz)

Offset 41 – BIOS ROM Decode Control (00h) .... RW

Setting these bits to 1 enables the indicated address range to be included in the ROMCS# decode:

- **7 000E0000h-000EFFFFh** .... default=0 (disable)
- **6 FFF00000h-FFF7FFFFh** .... default=0 (disable)
- **5 FFE80000h-FFEFFFFFh** .... default=0 (disable)
- **4 FFE00000h-FFE7FFFFh** .... default=0 (disable)
- **3 FFD80000h-FFDFFFFFh** .... default=0 (disable)
- **2 FFD00000h-FFD7FFFFh** .... default=0 (disable)
- **1 FFC80000h-FFCFFFFFh** .... default=0 (disable)
- **0 FFC00000h-FFC7FFFFh** .... default=0 (disable)

Note: ROMCS# is always active when ISA addresses FFF80000-FFFFFFFF and 000F0000-000FFFFF are decoded.

Offset 42 – Line Buffer Control (00h) .... RW

- **7 ISA Master DMA Line Buffer**
  Controls whether the DMA line buffer is used.
  - 0 Disable .... default
  - 1 Enable. Master DMA waits until the line buffer is full (8 DWords) before transmitting data (bit-6 must also be enabled to insure that there are no coherency issues).
- **6 Gate Interrupt Until Line Buffer Flush Complete**
  This bit should be enabled if bit-7 is enabled.
  - 0 Disable .... default
  - 1 Enable. IRQs are gated until the line buffer is flushed to insure that there are no coherency issues.
- **5 Flush Line Buffer for Interrupt**
  This bit controls whether the line bufer is flushed when an interrupt request is generated. This bit should be enabled if bit-7 is enabled.
  - 0 Disable .... default
  - 1 Enable
- **4 Uninterruptable Burst Read**
  - 0 Disable .... default
  - 1 Enable. The PCI bus is not granted to DMA until burst read transactions from the north bridge are completed.
- **3 Gate IRQ Until Line Bufer Flush Completed**
  - 0 Disable .... default
  - 1 Enable
- **2-0 Reserved** .... always reads 0

Offset 43 – Delay Transaction Control (00h) .... RW

- **7-4 Reserved (Do Not Program)** .... default = 0
- **3 Delayed Transactions (PCI Spec Rev 2.1)**
  This bit controls whether delayed transactions (delayed read / write and posted write) are enabled.
  - 0 Disable .... default
  - 1 Enable
- **2 Only Posted Write**
  This bit controls whether posted write is enabled, as opposed to bit-3 which controls whether delayed read / write as well as posted write are enabled.
  - 0 Disable .... default
  - 1 Enable
- **1 Write Delay Transaction Timeout Timer**
  When enabled, if a delayed transaction (write cycle only) is not retried after 2^{12} PCI clocks, the transaction is terminated.
  - 0 Disable .... default
  - 1 Enable
- **0 Read Delay Transaction Timeout Timer**
  When enabled, if a delayed transaction (read cycle only) is not retried after 2^{12} PCI clocks, the transaction is terminated.
  - 0 Disable .... default
  - 1 Enable

Offset 48 – Read Pass Write Control .... RW

7 APIC FSB Fixed at Low DW
- 0 Disable (Address Bit-2 not masked)...... default
- 1 Enable (force A2 from APIC FSB to low)

Address bit A2 controls whether data is in the lower (0) or upper (1) doubleword of a quadword sent to the CPU. When this bit is enabled, A2 is masked which means it is always 0 to select the lower doubleword.

6-4 Reserved .... always reads 0

3 AC97 / LPC Read Pass Write
- 0 Disable (a read cannot be performed before a preceeding write has been completed) .. default
- 1 Enable (internal AC97 and LPC devices are allowed to perform a read before a preceeding write)

2 IDE Read Pass Write
- 0 Disable (a read cannot be performed before a preceeding write has been completed) .. default
- 1 Enable (the internal IDE controller is allowed to perform a read before a preceeding write)

1 USB Read Pass Write
- 0 Disable (a read cannot be performed before a preceeding write has been completed) .. default
- 1 Enable (the internal USB controllers are allowed to perform a read before a preceeding write)

0 NIC Read Pass Write
- 0 Disable (a read cannot be performed before a preceeding write has been completed) .. default
- 1 Enable (the internal LAN controller is allowed to perform a read before a preceeding write)

Offset 49 – CCA Control .... RW

7 Reserved .... always reads 0

6 South Bridge Internal Master Devices Priority Higher Than External PCI Master
- 0 Disable .... default
- 1 Enable

The "CCA" is an internal arbiter that controls the priority of external PCI masters vs. internal master devices. Normally priority is the same for internal and external PCI master devices, but when this bit is enabled, internal master devices are given higher priority than external PCI masters (3/4 : 1/4).

5 CCA Clean to Mask Off IRQ

Controls whether interrupt requests are gated until data is written to memory.
- 0 Disable .... default
- 1 Enable

4-3 Reserved (Do Not Program) .... default = 0

2 WSC Mask Off INTR

Controls whether INTR is masked until write snoop is complete.
- 0 Disable .... default
- 1 Enable

1-0 Reserved (Do Not Program) .... default = 0

Miscellaneous Control

Offset 4C - IDE Interrupt Routing (04h) ....RW

7-6 I/O Recovery Time Select
When Rx40[6] is enabled, this field determines the I/O recovery time.
- 00 1 Bus Clock .... default
- 01 2 Bus Clock
- 10 4 Bus Clock
- 11 8 Bus Clock

5-4 Reserved (do not program) .... default = 0

3-2 IDE Secondary Channel IRQ Routing
- 00 IRQ14
- 01 IRQ15.. default
- 10 IRQ10
- 11 IRQ11

1-0 IDE Primary Channel IRQ Routing
- 00 IRQ14.. default
- 01 IRQ15
- 10 IRQ10
- 11 IRQ11

Note: IRQ Routing to the APIC is fixed as follows:

INTA# => IRQ16
INTB# => IRQ17
INTC# => IRQ18
INTD# => IRQ19
IDE IRQ => IRQ20
USB1 IRQ => IRQ21
USB2 IRQ => IRQ21 if Rx59[5] = 0
=> IRQ23 if Rx59[5] = 1
AC97 / MC97 IRQ => IRQ22

Table 10. APIC Fixed IRQ Routing

Offset 4E - Internal RTC Test Mode.............................. RW

7-5 Reserved .... always reads 0

4 Last Port 70/74 Written Status
- 0 Last write was to port 70 .... default
- 1 Last write was to port 74

3 Extra RTC Port 74/75
The RTC is normally accessed though ports 70/74. This bit controls whether two extra ports (74 / 75) can be used to access the RTC.
- 0 Disable .... default
- 1 Enable

2-0 Reserved (Do Not Program) .... default = 0

Offset 4F – PCI Bus and CPU Interface Control........... RW

7-4 Reserved .... always reads 0

3 CPU Reset Source
This bit determines whether CPU Reset (generated through port 92 or the keyboard) uses INIT or CPURST.
- 0 Use CPURST as CPU Reset .... default
- 1 Use INIT as CPU Reset

2 Reserved (Do Not Program) .... default = 0

1 Reserved .... always reads 0

0 Software PCI Reset ...... write 1 to generate PCI reset

Function Control

Offset 50 – Function Control 1 (09h) ....RW

- **7 Device 17 Function 6 MC97**
  - 0 Enable.. default
  - 1 Disable
- **6 Device 17 Function 5 AC97**
  - 0 Enable.. default
  - 1 Disable
- **5 Device 16 Function 1 USB 1.1 UHCI Ports 2-3**
  - 0 Enable.. default
  - 1 Disable
- **4 Device 16 Function 0 USB 1.1 UHCI Ports 0-1**
  - 0 Enable.. default
  - 1 Disable
- **3 Device 17 Function 1 IDE**
  - 0 Enable
  - 1 Disable **...default**
- **2 Device 16 Function 2 USB 1.1 UHCI Ports 4-5**
  - 0 Enable.. default
  - 1 Disable
- **1 Device 16 Function 4 USB 2.0 EHCI**
  - 0 Enable.. default
  - 1 Disable
- **0 Internal Audio .... RO**
  - 0 Disable
  - 1 Enable**...default**

Offset 51 – Function Control 2 (0Dh)............................. RW

- **7-6 Reserved** .... always reads 0
- **5 Internal LAN Controller Clock Gating**
  When bit-4 of this register is disabled, the LAN function is disabled but the LAN controller clock is not gated automatically. This bit controls whether the clock is actually gated.
  - 0 Disable .... default
  - 1 Enable
- **4 Internal LAN Controller**
  - 0 Disable .... default
  - 1 Enable
- **3 Internal RTC**
  - 0 Disable
  - 1 Enable **... default**
- **2 Internal PS2 Mouse**
  - 0 Disable
  - 1 Enable **... default**
- **1 Internal KBC Configuration**
  - 0 Disable ports 2E / 2F offsets E0-EF ...... default
  - 1 Enable ports 2E / 2F offsets E0-EF
- **0 Internal KBC**
  - 0 Disable
  - 1 Enable **... default**

Pin	0 / Disable (External KBC)	1 / Enable (Internal KBC)
AF12	KBCS#	ROMCS#
V2	KBRC	KBDT
V3	KA20G	KBCK
W1	IRQ12	MSDT
W2	IRQ1	MSCK

Serial IRQ, LPC, and PC/PCI DMA Control

Offset 52 – Serial IRQ & LPC Control (00h)..................RW

- **7 Reserved** .... always reads 0
- **6 LPC Short Wait Abort**
  - 0 Disable .... default
  - 1 Enable. During a short wait, the cycle is aborted after 8Ts.
- **5 LPC Frame Wait State Time**
  - 0 Frame Wait State is 1T.......................... default
  - 1 Frame Wait State is 2T
- **4 LPC Stop to Start Frame Wait State**
  - 0 Enable. One idle state is inserted between Stop and Start .... default
  - 1 Disable. Stop is followed immediately by Start.
- **3 Serial IRQ**
  - 0 Disable .... default
  - 1 Enable (IRQ asserted via SerialIRQ pin AE10)
- **2 Serial IRQ Quiet Mode**
  - 0 Continuous Mode .... default
  - 1 Quiet Mode
- **1-0 Serial IRQ Start-Frame Width**
  - 00 4 PCI Clocks .... default
  - 01 6 PCI Clocks
  - 10 8 PCI Clocks
  - 11 10 PCI Clocks

Offset 53 – PC/PCI DMA Control ....RW

- **7 PCI DMA Pair A and Pair B**
  - 0 Disable .... default
  - 1 Enable
- **6 PCI DMA Channel 7**
  - 0 Disable .... default
  - 1 Enable
- **5 PCI DMA Channel 6**
  - 0 Disable .... default
  - 1 Enable
- **4 PCI DMA Channel 5**
  - 0 Disable .... default
  - 1 Enable
- **3 PCI DMA Channel 3**
  - 0 Disable .... default
  - 1 Enable
- **2 PCI DMA Channel 2**
  - 0 Disable .... default
  - 1 Enable
- **1 PCI DMA Channel 1**
  - 0 Disable .... default
  - 1 Enable
- **0 PCI DMA Channel 0**
  - 0 Disable .... default
  - 1 Enable

Plug and Play Control - PCI

Offset 54 - PCI Interrupt Polarity.................................. RW

- **7-4 Reserved** ....always reads 0

The following bits all default to “level” triggered (0)

- **3 PCI INTA# Invert (edge) / Non-invert (level)** . (1/0)
- **2 PCI INTB# Invert (edge) / Non-invert (level)** . (1/0)
- **1 PCI INTC# Invert (edge) / Non-invert (level)** . (1/0)
- **0 PCI INTD# Invert (edge) / Non-invert (level)** . (1/0)

Note: PCI INTA-D# normally connect to PCI interrupt pins INTA-D# (see pin definitions for more information).

Offset 55 – PCI PNP Interrupt Routing 1 .... RW

- **7-4 PCI INTA# Routing** (see PnP IRQ routing table)
- **3-0 Reserved** ....always reads 0

Offset 56 – PCI PNP Interrupt Routing 2 .... RW

- **7-4 PCI INTC# Routing** (see PnP IRQ routing table)
- **3-0 PCI INTB# Routing** (see PnP IRQ routing table)

Offset 57 – PCI PNP Interrupt Routing 3 .... RW

- **7-4 PCI INTD# Routing** (see PnP IRQ routing table)
- **3-0 Reserved** ....always reads 0

Table 11. PnP IRQ Routing Table

0000	Disabled .... default
0001	IRQ1
0010	Reserved
0011	IRQ3
0100	IRQ4
0101	IRQ5
0110	IRQ6
0111	IRQ7
1000	Reserved
1001	IRQ9
1010	IRQ10
1011	IRQ11
1100	IRQ12
1101	Reserved
1110	IRQ14
1111	IRQ15

GPIO and Miscellaneous Control

Offset 58 – Miscellaneous Control 0 (40h)......................RW

- **7 Reserved** .... always reads 0
- **6 Internal APIC**
  - 0 Disable
  - 1 Enable**...default**
- **5 South Bridge Interrupt Cycles Run at 33 MHz**
  - 0 Disable .... default
  - 1 Enable
- **4 Address Decode**
  - 0 Subtractive... default
  - 1 Positive
- **3 RTC High Bank Access**
  - 0 Disable access to upper 128 bytes......... default
  - 1 Enable access to upper 128 bytes
- **2 RTC Rx32 Write Protect**
  - 0 Disable (not protected).......................... default
  - 1 Enable (write protected)
- **1 RTC Rx0D Write Protect**
  - 0 Disable (not protected).......................... default
  - 1 Enable (write protected)
- **0 RTC Rx32 Map to Century Byte**
  Controls whether RTC Rx32 is mapped to the century byte.
  - 0 Disable .... default
  - 1 Enable

Offset 59 – Miscellaneous Control 1 (00h)..................... RW

- **7-6 Reserved** ....always reads 0
- **5 LPC RTC**
  - 0 Disable... default
  - 1 Enable
- **4 LPC Keyboard**
  - 0 Disable (ISA Keyboard) .... default
  - 1 Enable (LPC Keyboard)
- **3 External MCCS to LPC**
  Controls whether external MCCS is through LPC or ISA when internal MCCS is not used.
  - 0 Disable (ISA MCCS)............................ default
  - 1 Enable (LPC MCCS)
- **2 Internal MCCS (Microcontroller Chip Select)**
  - 0 Disable (external MCCS) .... default
  - 1 Enable (internal MCCS)
- **1 A20M# Active**
  - 0 Disable (A20M# signal not asserted)..... default
  - 1 Enable (A20M# signal asserted)
- **0 NMI on PCI Parity Error**
  - 0 Disable... default
  - 1 Enable (to generate NMI, Port 61[3] and Port 70[7] must also be set)

Offset 5A – DMA Bandwidth Control (00h) ....RW

7 DMA Channel 7 Bandwidth
- 0 Normal .... default
- 1 Improved

6 DMA Channel 6 Bandwidth
- 0 Normal .... default
- 1 Improved

5 DMA Channel 5 Bandwidth
- 0 Normal .... default
- 1 Improved

4 DMA Single Transfer Mode Bandwidth
- 0 Normal .... default
- 1 Improved

3 DMA Channel 3 Bandwidth
- 0 Normal .... default
- 1 Improved

2 DMA Channel 2 Bandwidth
- 0 Normal .... default
- 1 Improved

1 DMA Channel 1 Bandwidth
- 0 Normal .... default
- 1 Improved

0 DMA Channel 0 Bandwidth
- 0 Normal .... default
- 1 Improved

The above bits determine if DMA bandwidth is improved for the specified channel. If enabled, bandwidth improvement is accomplished by reducing the transaction latency between the DMA Controller and the LPC Bus Controller.

Offset 5B – Miscellaneous Control 2 (01h) .... RW

7-4 Reserved ....always reads 0

3 Bypass APIC De-Assert Message
- 0 Disable .... default
- 1 Enable

2 APIC HyperTransport Mode
- 0 Disable .... default
- 1 Enable

1 INTE#, INTF#, INTG#, INTH# (pins GPIO12-15)
- 0 Disable .... default
- 1 Enable

0 Dynamic Clock Stop
- 0 Disable
- 1 Enable **.. default**

Programmable Chip Select Control

Offset 5D-5C – PCS 0 I/O Port Address (0000h)............RW

15-0 PCS 0 I/O Port Address.......................... default = 0

Offset 5F-5E – PCS 1 I/O Port Address (0000h).............RW

15-0 PCS 1 I/O Port Address.......................... default = 0

Offset 61-60 – PCS 2 I/O Port Address (0000h)..............RW

15-0 PCS 2 I/O Port Address.......................... default = 0

Offset 63-62 – PCS 3 I/O Port Address (0000h)..............RW

15-0 PCS 3 I/O Port Address.......................... default = 0

Offset 65-64 – PCS I/O Port Address Mask (0000h) ......RW

15-12 PCS 3 I/O Port Address Mask 3-0
- 0000 Decode range is 1 byte .... default
- 0001 Decode range is 2 bytes
- 0011 Decode range is 4 bytes
- 0111 Decode range is 8 bytes
- 1111 Decode range is 16 bytes

11-8 PCS 2 I/O Port Address Mask 3-0
- 0000 Decode range is 1 byte .... default
- 0001 Decode range is 2 bytes
- 0011 Decode range is 4 bytes
- 0111 Decode range is 8 bytes
- 1111 Decode range is 16 bytes

7-4 PCS 1 I/O Port Address Mask 3-0
- 0000 Decode range is 1 byte .... default
- 0001 Decode range is 2 bytes
- 0011 Decode range is 4 bytes
- 0111 Decode range is 8 bytes
- 1111 Decode range is 16 bytes

3-0 PCS 0 I/O Port Address Mask 3-0
- 0000 Decode range is 1 byte .... default
- 0001 Decode range is 2 bytes
- 0011 Decode range is 4 bytes
- 0111 Decode range is 8 bytes
- 1111 Decode range is 16 bytes

Offset 66 – PCS Control (00h) .... RW

7 PCS 3 Internal I/O
- 0 Disable (External)................................. default
- 1 Enable (Internal)

6 PCS 2 Internal I/O
- 0 Disable (External)................................. default
- 1 Enable (Internal)

5 PCS 1 Internal I/O
- 0 Disable (External)................................. default
- 1 Enable (Internal)

4 PCS 0 Internal I/O
- 0 Disable (External)................................. default
- 1 Enable (Internal)

The above 4 bits determine whether Programmable Chip Selects 0-3 are treated as internal I/O

3 PCS 3
- 0 Disable .... default
- 1 Enable

2 PCS 2
- 0 Disable .... default
- 1 Enable

1 PCS 1
- 0 Disable .... default
- 1 Enable

0 PCS 0
- 0 Disable .... default
- 1 Enable

Offset 67 – Output Control (04h) .... RW

7-3 Reserved .... always reads 0

2 FERR Voltage
- 0 2.5V
- 1 1.5V **... default**

1-0 Reserved .... always reads 0

ISA Decoding Control

Offset 6C – ISA Positive Decoding Control 1..................RW

7 On-Board I/O (Ports 00-FFh) Positive Decoding
- 0 Disable .... default
- 1 Enable

6 Microsoft-Sound System I/O Port Positive Decoding
- 0 Disable .... default
- 1 Enable (bits 5-4 determine the decode range)

5-4 Microsoft Sound System I/O Decode Range
- 00 0530h-0537h .... default
- 01 0604h-060Bh
- 10 0E80-0E87h
- 11 0F40h-0F47h

3 Internal APIC Positive Decoding
- 0 Disable .... default
- 1 Enable

2 BIOS ROM Positive Decoding
- 0 Disable .... default
- 1 Enable

1 Internal PCS1# Positive Decoding
- 0 Disable .... default
- 1 Enable

0 Internal PCS0# Positive Decoding
- 0 Disable .... default
- 1 Enable

Offset 6D – ISA Positive Decoding Control 2..................RW

7 FDC Positive Decoding
- 0 Disable .... default
- 1 Enable

6 LPT Positive Decoding
- 0 Disable .... default
- 1 Enable

5-4 LPT Decode Range
- 00 3BCh-3BFh, 7BCh-7BEh..................... default
- 01 378h-37Fh, 778h-77Ah
- 10 278h-27Fh, 678h-67Ah
- 11 -reserved-

3 Game Port Positive Decoding
- 0 Disable .... default
- 1 Enable

2 MIDI Positive Decoding
- 0 Disable .... default
- 1 Enable

1-0 MIDI Decode Range
- 00 300-303h .... default
- 01 310-313h
- 10 320-323h
- 11 330-333h

Offset 6E – ISA Positive Decoding Control 3 .... RW

7 COM Port B Positive Decoding
- 0 Disable .... default
- 1 Enable

6-4 COM-Port B Decode Range
- 000 3F8h-3FFh (COM1)........................... default
- 001 2F8h-2FFh (COM2)
- 010 220h-227h
- 011 228h-22Fh
- 100 238h-23Fh
- 101 2E8h-2EFh (COM4)
- 110 338h-33Fh
- 111 3E8h-3EFh (COM3)

3 COM Port A Positive Decoding
- 0 Disable .... default
- 1 Enable

2-0 COM-Port A Decode Range
- 000 3F8h-3FFh (COM1)........................... default
- 001 2F8h-2FFh (COM2)
- 010 220h-227h
- 011 228h-22Fh
- 100 238h-23Fh
- 101 2E8h-2EFh (COM4)
- 110 338h-33Fh
- 111 3E8h-3EFh (COM3)

Offset 6F – ISA Positive Decoding Control 4 .... RW

7-6 Reserved .... always reads 0

5 PCS2# and PCS3# Positive Decoding
- 0 Disable .... default
- 1 Enable

4 I/O Port 0CF9h Positive Decoding
- 0 Disable .... default
- 1 Enable

3 FDC Decoding Range
- 0 Primary .... default
- 1 Secondary

2 Sound Blaster Positive Decoding
- 0 Disable .... default
- 1 Enable

1-0 Sound Blaster Decode Range
- 00 220-233h.. default
- 01 240-253h
- 10 260-273h
- 11 280-293h

I/O Pad Control

Offset 7C – I/O Pad Control (00h) ....RW

- **7-6 Reserved** .... always reads 0
- **5-4 IDE Interface Output Drive Strength**
  - 00 Lowest .... default
  - … …
  - 11 Highest
- **3-2 PLL PCLK Input Delay Select**
  - 00 .... default
  - … …
  - 11
- **1-0 PLL CLK66 Feedback Delay Select**
  - 00 .... default
  - … …
  - 11

Power Management-Specific Configuration Registers

Offset 80 – General Configuration 0 (00h)......................RW

- **7 Reserved** .... always reads 0
- **6 Sleep Button**
  - 0 Disable .... default
  - 1 Sleep Button is on GPI21 / ACSDIN3 pin (V1)
- **5 Debounce LID and PWRBTN# Inputs for 200us**
  This bit controls whether the debounce circuit for the LID# and PWRBTN# inputs is enabled to reduce possible noise.
  - 0 Disable .... default
  - 1 Enable
- **4 Reserved (Do Not Program)**.................... default = 0
- **3 Microsoft Sound Monitor in Audio Access**
  This bit controls whether an I/O access to the sound port sets I/O Rx33-30[10] (Audio Access Status) = 1.
  - 0 Disable .... default
  - 1 Enable
- **2 Game Port Monitor in Audio Access**
  This bit controls whether an I/O access to the game port sets I/O Rx33-30[10] (Audio Access Status) = 1.
  - 0 Disable .... default
  - 1 Enable
- **1 Sound Blaster Monitor in Audio Access**
  This bit controls whether an I/O access to the sound blaster port sets I/O Rx33-30[10] (Audio Access Status) = 1.
  - 0 Disable .... default
  - 1 Enable
- **0 MIDI Monitor in Audio Access**
  This bit controls whether an I/O access to the MIDI port sets I/O Rx33-30[10] (Audio Access Status) = 1.
  - 0 Disable .... default
  - 1 Enable

Offset 81 - General Configuration 1 (04h)...................... RW

- **7 I/O Enable for ACPI I/O Base**
  - 0 Disable access to ACPI I/O block.......... default
  - 1 Allow access to Power Management I/O Register Block (see offset 4B-48 to set the base address for this register block). The definitions of the registers in the Power Management I/O Register Block are included later in this document, following the Power Management Subsystem overview.
- **6-4 Reserved** ....always reads 0
- **3 ACPI Timer Count Select**
  - 0 24-bit Timer... default
  - 1 32-bit Timer
- **2 RTC Enable Signal Gated with PSON (SUSC#) in Soft-Off Mode**
  This bit controls whether RTC control signals are gated during system suspend state. This is to prevent CMOS and Power-Well register data from being corrupted during system on/off when the control signals (PWRGD) may not be stable.
  - 0 Disable
  - 1 Enable **.. default**
- **1 Clock Throttling Clock Select (STPCLK#)**
  This bit controls the timer tick base for the throttle timer.
  - 0 30 usec (480 usec cycle time when using a 4-bit timer) .... default
  - 1 1 msec (16 msec cycle time when using a 4-bit timer)

  The timer tick base can be further lowered to 7.5 usec (120 usec cycle time when using a 4-bit timer) by setting Rx8D[4] = 1. When Rx8D[4] = 1, the setting of this bit is ignored.
- **0 Reserved (Do Not Program)** ....default = 0

Offset 82 - ACPI Interrupt Select ....RW

7 ATX / AT Power Indicator .... **RO**
- 0 ATX
- 1 AT

6 PSON (SUSC#) Gating .... **RO**
During system on/off, this status bit reports whether PSON gating state has been completed, 0 meaning that gating is active now and 1 meaning that gating is complete. Software should not access any CMOS or Power-Well registers until this bit becomes 1 if Rx81[2] = 1 (see register description on previous page).
- 0 PSON Gating Active
- 1 PSON Gating Complete

5 Reserved .... always reads 0

4 SUSC# AC-Power-On Default Value .... **RO**
This bit is written at RTC Index 0D bit-7. If this bit is 0, the system is configured to "default on" when power is connected.

3-0 SCI Interrupt Assignment
This field determines the routing of the ACPI IRQ.
- 0000 Disabled.. default
- 0001 IRQ1
- 0010 Reserved
- 0011 IRQ3
- 0100 IRQ4
- 0101 IRQ5
- 0110 IRQ6
- 0111 IRQ7
- 1000 IRQ8
- 1001 IRQ9
- 1010 IRQ10
- 1011 IRQ11
- 1100 IRQ12
- 1101 IRQ13
- 1110 IRQ14
- 1111 IRQ15

Offset 85-84 - Primary Interrupt Channel (0000h) ....RW

If a device IRQ is enabled as a Primary IRQ, that device's IRQ can be used to generate wake events. The bits in this register are used in conjunction with:

- PMIO Rx28[7] – Primary Resume Status
- PMIO Rx2A[7] – Primary Resume Enable

If a device on one of the IRQ's is set to enable the Primary Interrupt, once the device generates an IRQ, the PMIO Rx28[7] status bit will become 1 to report the occurrence of the Primary IRQ. If PMIO Rx2A[7] is set to 1 to enable Resume-on-Primary-IRQ, the IRQ then becomes a wake event.

15	**1/0 = Ena/Disa IRQ15 as Primary Intrpt Channel**
14	**1/0 = Ena/Disa IRQ14 as Primary Intrpt Channel**
13	**1/0 = Ena/Disa IRQ13 as Primary Intrpt Channel**
12	**1/0 = Ena/Disa IRQ12 as Primary Intrpt Channel**
11	**1/0 = Ena/Disa IRQ11 as Primary Intrpt Channel**
10	**1/0 = Ena/Disa IRQ10 as Primary Intrpt Channel**
9	**1/0 = Ena/Disa IRQ9 as Primary Intrpt Channel**
8	**1/0 = Ena/Disa IRQ8 as Primary Intrpt Channel**
7	**1/0 = Ena/Disa IRQ7 as Primary Intrpt Channel**
6	**1/0 = Ena/Disa IRQ6 as Primary Intrpt Channel**
5	**1/0 = Ena/Disa IRQ5 as Primary Intrpt Channel**
4	**1/0 = Ena/Disa IRQ4 as Primary Intrpt Channel**
3	**1/0 = Ena/Disa IRQ3 as Primary Intrpt Channel**
2	**Reserved** .... always reads 0
1	**1/0 = Ena/Disa IRQ1 as Primary Intrpt Channel**
0	**1/0 = Ena/Disa IRQ0 as Primary Intrpt Channel**

Offset 87-86 - Secondary Interrupt Channel (0000h) .... RW

For legacy PMU, the bits in this register are used in conjunction with:

- PMIO Rx28[1] – Secondary Event Timer Timeout Status
- PMIO Rx2A[7] – SMI on Secondary Event Timer Timeout

Secondary IRQ's are different from Primary IRQ's in that systems that resume due to a Secondary IRQ can return directly to suspend state after the secondary event timer times out. For this to work, PMIO Rx2A[1] needs to be set to one to enable SMI-on-Secondary-Event-Timer-Timeout (when PMIO Rx28[1] = 1). The timer's count value can be set via Rx93-90[27-26].

15	**1/0 = Ena/Disa IRQ15 as Secondary Intr Channel**
14	**1/0 = Ena/Disa IRQ14 as Secondary Intr Channel**
13	**1/0 = Ena/Disa IRQ13 as Secondary Intr Channel**
12	**1/0 = Ena/Disa IRQ12 as Secondary Intr Channel**
11	**1/0 = Ena/Disa IRQ11 as Secondary Intr Channel**
10	**1/0 = Ena/Disa IRQ10 as Secondary Intr Channel**
9	**1/0 = Ena/Disa IRQ9 as Secondary Intr Channel**
8	**1/0 = Ena/Disa IRQ8 as Secondary Intr Channel**
7	**1/0 = Ena/Disa IRQ7 as Secondary Intr Channel**
6	**1/0 = Ena/Disa IRQ6 as Secondary Intr Channel**
5	**1/0 = Ena/Disa IRQ5 as Secondary Intr Channel**
4	**1/0 = Ena/Disa IRQ4 as Secondary Intr Channel**
3	**1/0 = Ena/Disa IRQ3 as Secondary Intr Channel**
2	**Reserved** .... always reads 0
1	**1/0 = Ena/Disa IRQ1 as Secondary Intr Channel**
0	**1/0 = Ena/Disa IRQ0 as Secondary Intr Channel**

Offset 8B-88 – Power Management I/O Base..................RW

31-16 Reserved .... always reads 0

15-7 Power Management I/O Register Base Address
Port Address for the base of the 128-byte Power Management I/O Register block, corresponding to AD[15:7]. See "Power Management I/O Space Registers" in this document for definitions of the registers in the Power Management I/O Register Block

6-0 0000001b

Offset 8C – Host Bus Power Management Control........RW

7-4 Thermal Duty Cycle
This field determines the duty cycle of STPCLK# when the THRM# pin is asserted. The duty cycle indicates the percentage of performance (the lower the percentage, the lower the performance and the higher the power savings). The STPCLK# duty cycle when THRM# is NOT asserted is controlled by PMIO Rx10[3:0]. If the setting in that field is lower than the setting in this field, the lower setting will be used for thermal duty cycle.

0000 Reserved .... default
0001 0-6.25%
0010 6.25-12.50%
0011 18.75-25.00%
0100 31.25-37.50%
0101 37.50-43.75%
0110 43.75-50.00%
0111 50.00-56.25%
1000 56.25-62.50%
1001 62.50-68.75%
1010 68.75-75.00%
1011 75.00-87.50%
1100 75.00-81.25%
1101 81.25-87.50%
1110 87.50-93.75%
1111 93.75-100%

3 THRM Enable
0 Disable .... default
1 Enable

2 Processor Break Event
0 Disable .... default
1 Enable

1-0 Reserved .... always reads 0

Offset 8D – Throttle / Clock Stop Control...................... RW

7 Throttle Timer Reset..................................... def = 0

6-5 Throttle Timer
This field determines the number of bits used for the throttle timer, which in conjunction with the throttle timer tick determines the cycle time of STPCLK#. For example, if a 2-bit timer and a 7.5 usec timer tick are selected, the STPCLK# cycle time would be 30 usec (2**2 x 7.5). If a 4-bit timer and a 7.5 usec timer tick is selected, the cycle time would be 120 usec (2**4 x 7.5).

0x 4-Bit .... default
10 3-Bit
11 2-Bit

4 Fast Clock (7.5us) as Throttle Timer Tick
This bit controls whether the throttle timer tick uses 7.5 usec as its time base (120 usec cycle time when using a 4-bit timer).

0 Timer Tick is selected by Rx80[1] .... default
1 Timer Tick is 7.5 usec (Rx80[1] is ignored)

3 SMI Level Output (Low)
0 Disable .... default
1 Enable (during an SMI event, SMI# is held low until SMI event status is cleared)

2 Internal Clock Stop for PCI Idle
This bit controls whether the internal PCI clock is stopped when PCKRUN# is high.

0 PCI clock is not stopped .... default
1 PCI clock is stopped

1 Internal Clock Stop During C3
This bit controls whether the internal PCI clock is stopped during C3 state.

0 PCI clock is not stopped .... default
1 PCI clock is stopped

0 Internal Clock Stop During Suspend
This bit controls whether the internal PCI clock is stopped during Suspend state.

0 PCI clock is not stopped .... default
1 PCI clock is stopped

Offset 93-90 - GP Timer Control (0000 0000h)...............RW

31-30 Conserve Mode Timer Count Value
- 00 1/16 second.. default
- 01 1/8 second
- 10 1 second
- 11 1 minute

29 Conserve Mode Status
This bit reads 1 when in Conserve Mode

28 Conserve Mode
This bit controls whether conserve mode (throttling) is enabled. When this bit is set, the system can enter conserve mode when primary activity is not detected within a given time period (determined by bits 31-30 of this register). Primary activity is defined in PMIO Rx33-30.
- 0 Disable .... default
- 1 Enable

27-26 Secondary Event Timer Count Value
- 00 2 milliseconds....................................... default
- 01 64 milliseconds
- 10 ½ second
- 11 by EOI + 0.25 milliseconds

25 Secondary Event Occurred Status
This bit reads 1 to indicate that a secondary event has occurred (to resume the system from suspend) and the secondary event timer is counting down.

24 Secondary Event Timer Enable
- 0 Disable .... default
- 1 Enable

23-16 GP1 Timer Count Value (base defined by bits 5-4)
Write to load count value; Read to get current count

15-8 GP0 Timer Count Value (base defined by bits 1-0)
Write to load count value; Read to get current count

7 GP1 Timer Start
On setting this bit to 1, the GP1 timer loads the value defined by bits 23-16 of this register and starts counting down. The GP1 timer is reloaded at the occurrence of certain peripheral events enabled in the GP Timer Reload Enable Register (Power Management I/O Space Offset 38h). If no such event occurs and the GP1 timer counts down to zero, then the GP1 Timer Timeout Status bit is set to one (bit-3 of the Global Status register at Power Management Register I/O Space Offset 28h). Additionally, if the GP1 Timer Timeout Enable bit is set (bit-3 of the Global Enable register at Power Management Register I/O Space Offset 2Ah), then an SMI is generated.

6 GP1 Timer Automatic Reload
- 0 GP1 Timer stops at 0 ....default
- 1 Reload GP1 timer automatically after counting down to 0

5-4 GP1 Timer Base
- 00 Disable..default
- 01 1/16 second
- 10 1 second
- 11 1 minute

3 GP0 Timer Start
On setting this bit to 1, the GP0 timer loads the value defined by bits 15-8 of this register and starts counting down. The GP0 timer is reloaded at the occurrence of certain peripheral events enabled in the GP Timer Reload Enable Register (Power Management I/O Space Offset 38h). If no such event occurs and the GP0 timer counts down to zero, then the GP0 Timer Timeout Status bit is set to one (bit-2 of the Global Status register at Power Management Register I/O Space Offset 28h). Additionally, if the GP0 Timer Timeout Enable bit is set (bit-2 of the Global Enable register at Power Management Register I/O Space Offset 2Ah), then an SMI is generated.

2 GP0 Timer Automatic Reload
- 0 GP0 Timer stops at 0 ....default
- 1 Reload GP0 timer automatically after counting down to 0

1-0 GP0 Timer Base
- 00 Disable..default
- 01 1/16 second
- 10 1 second
- 11 1 minute

Offset 94 – Power Well Control .... WO

7 SMBus Clock Select
- 0 SMBus Clock from 14.31818 MHz Divider
- 1 SMBus Clock from RTC 32.768 KHz ... defult

6 Reserved .... always reads 0

5 Internal PLL Reset During Suspend
- 0 Enable.. default
- 1 Disable

4 SUSST1# / GPO3 Select (Pin Y3)
- 0 SUSST1#... default
- 1 GPO3

3 GPO2 / SUSB# Select (Pin AF2)
- 0 SUSB#.. default
- 1 GPO2

2 GPO1 / SUSA# Select (Pin AA2)
- 0 SUSA# .... default
- 1 GPO1

1-0 GPO0 Output Select (Pin AA3)
This field controls the GPO0 output signal for Pulse Width Modulation.
- 00 GPO0 Fixed Output Level (defined by PMIO Rx4C[0]) .... default
- 01 GPO0 output is 1 Hz "SLOWCLK"
- 10 GPO0 output is 4 Hz "SLOWCLK"
- 11 GPO0 output is 16 Hz "SLOWCLK"

Offset 95 – Miscellaneous Power Well Control............. RW

7 CPUSTP# to SUSST# Delay Select
This bit controls the delay between the deassertion of CPUSTP# and the deassertion of SUSST# during a resume.
- 0 1 msec minimum .... default
- 1 125 usec minimum

6 SUSST# Deasserted Before PWRGD for STD
- 0 Disable... default
- 1 Enable (SUST# is deasserted before PWRGD when resuming from STD)

5 Keyboard / Mouse Port Swap
This bit determines whether the keyboard and mouse ports can be swapped.
- 0 Disable... default
- 1 Enable

4 Reserved .... always reads 0

3 SMB2 / GPO Select
- 0 SMBDT2 / SMBCK2 .... default
- 1 GPO26 / GPO27

2 AOL 2 SMB Slave
This bit controls whether external SMB masters can access internal SMB registers (for Alert-On-LAN).
- 0 Enable (external SMB masters may reset / resume the system (when Rx96[4]=1) or detect GPI status) .... default
- 1 Disable

1 SUSCLK / GPO4 Select
- 0 SUSCLK... default
- 1 GPO4

0 USB Wakeup for STR / STD / SoftOff
This bit controls whether USB Wakeup is enabled when PMIO Rx21-20[14] (USB Wakeup Status) = 1. This allows wakeup from STR, STD, Soft Off, and POS.
- 0 Disable... default
- 1 Enable

Offset 96 – Power On / Reset Control .... RW

7-4 Reserved .... always reads 0

3-0 CPU Frequency Strapping Value Output to NMI, INTR, IGNNE#, and A20M# during RESET#
The value written to this field is strapped through NMI, INTR, IGNNE#, and A20M# during RESET# to determine the multiplier for setting the CPU's internal frequency. If the CPU hangs due to inappropriate settings written here, the GP3 timer (second timeout) can be used to initiate a system reboot (PMIO Rx42[2] = 1). Refer to the BIOS Porting Guide for additional details.

Offset 98 – GP2 / GP3 Timer Control ....RW

7 GP3 Timer Start
On setting this bit to 1, the GP3 timer loads the value defined by Rx5A and starts counting down. The GP3 timer is reloaded at the occurrence of certain events enabled in the GP Timer Reload Enable Register (Power Management I/O Space Offset 38h). If no such event occurs and the GP3 timer counts down to zero, then the GP3 Timer Timeout Status bit is set to one (bit-13 of the Global Status register at Power Management Register I/O Space Offset 28h). Additionally, if the GP3 Timer Timeout Enable bit is set (bit-13 of the Global Enable register at Power Management Register I/O Space Offset 2Ah), then an SMI is generated.

6 GP3 Timer Automatic Reload
- 0 GP3 Timer stops at 0 .... default
- 1 Reload GP3 timer automatically after counting down to 0

5-4 GP3 Timer Tick Select
- 00 Disable .... default
- 01 1/16 second
- 10 1 second
- 11 1 minute

3 GP2 Timer Start
On setting this bit to 1, the GP2 timer loads the value defined by Rx59 and starts counting down. The GP2 timer is reloaded at the occurrence of certain events enabled in the GP Timer Reload Enable Register (Power Management I/O Space Offset 38h). If no such event occurs and the GP2 timer counts down to zero, then the GP2 Timer Timeout Status bit is set to one (bit-12 of the Global Status register at Power Management Register I/O Space Offset 28h). Additionally, if the GP2 Timer Timeout Enable bit is set (bit-12 of the Global Enable register at Power Management Register I/O Space Offset 2Ah), then an SMI is generated.

2 GP2 Timer Automatic Reload
- 0 GP2 Timer stops at 0 .... default
- 1 Reload GP2 timer automatically after counting down to 0

1-0 GP2 Timer Tick Select
- 00 Disable .... default
- 01 1/16 second
- 10 1 second
- 11 1 minute

Offset 99 – GP2 Timer.. RW

7 Write: GP2 Timer Load Value..............default = 0
Read: GP2 Timer Current Count

Offset 9A – GP3 Timer... RW

7 Write: GP3 Timer Load Value..............default = 0
Read: GP3 Timer Current Count

Offset C3-C0 – Power Management Capability............. RO

31-16 Power Management Capability.always reads 0002h
15-8 Next Pointer ....always reads 00h
7-0 Capability ID ....always reads 01h

Offset C7-C4 – Power Mgmt Capability CSR................ RW

31-24 Power Management Data..............always reads 00h
23-16 PM CSR P2P Support Extensions.always reads 00h
15-0 PM Control / Status (D0/D3 Only)..default = 0000h

System Management Bus-Specific Configuration Registers

Offset D1-D0 – SMBus I/O Base ....RW

- **15-4 I/O Base (16-byte I/O space)** .... default = 00h
- **3-0 Fixed** .... always reads 0001b

Offset D2 – SMBus Host Configuration ....RW

- **7-4 Reserved** .... always reads 0
- **3 SMBus Interrupt Type**
  - 0 SMI .... default
  - 1 SCI
- **2 Reserved** .... always reads 0
- **1 SMBus Interrupt Enable**
  - 0 Disable SCI / SMI .... default
  - 1 Enable SCI / SMI
- **0 SMBus Host Controller Enable**
  - 0 Disable SMB controller functions .... default
  - 1 Enable SMB controller functions

Offset D3 – SMBus Host Slave Command ....RW

- **7-0 SMBus Host Slave Command Code** .... default=0

Offset D4 – SMBus Slave Address for Port 1..................RW

- **7-1 SMBus Slave Address for Port 1**............... default=0
- **0 Read / Write for Shadow Port 1**

Offset D5 – SMBus Slave Address for Port 2..................RW

- **7-1 SMBus Slave Address for Port 2**............... default=0
- **0 Read / Write for Shadow Port 2**

Offset D6 – SMBus Revision ID .... RO

- **7-0 SMBus Revision Code**

SMB GPIO Slave Command Codes

SMBus Command Code 0 – GPIO Slave Input Port...... RO

- **7-0 Input Data** .... default per pins
  Reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output. Writes to this register have no effect.

SMBus Command Code 1 – GPIO Slave Output Port.. RW

- **7-0 Output Data** ....default = 0
  Controls the levels of the GPIO output pins defined as outputs. Bit values in this register have no effect on pins defined as inputs. Reads from this register reflect the saved value last written, not the actual pin value.

SMBus Cmd Code 2 – GPIO Slave Polarity Inversion.. RW

- **7-0 Polarity Inversion**................................default = 0Fh
  This register enables polarity inversion of pins defined as inputs by Command Code 3.
  - 0 Corresponding pin's polarity unchanged
  - 1 Corresponding pin's polarity inverted

SMBus Cmd Code 3 – GPIO Slave I/O Configuration.. RW

- **7-0 Input / Output Configuration**........... default = 0FFh
  This register configures the directions of the I/O pins.
  - 0 Corresponding pin is an output
  - 1 Corresponding pin is an input**.............. default**

General Purpose I/O Control Registers

Offset E0 – GPI Inversion Control ....RW

7-0 GPI[27-24, 19-16] Input Inversion
- 0 Non-inverted input .... default
- 1 Inverted input

Offset E1 – GPI SCI / SMI Select.....................................RW

7-0 GPI[27-24, 19-16] SCI / SMI Select
When GPI[27-24,19-16] are set to enable SCI / SMI generation (PMIO Rx52), this field determines whether an SCI or SMI is generated.
- 0 SCI .... default
- 1 SMI

Offset E4 – GPO Pin Select ....RW

7 Reserved .... always reads 0

6 ACSDIN2,3 / GPIO20,21 Select (Pins U2, V1)
This bit is ignored if any of RxE5 bits 1, 2, 4, or 5 = 1
- 0 U2 = ACSDIN2, V1 = ACSDIN3......... default
- 1 U2 = GPIO20, V1 = GPIO21

5 SA[19:16] / GPO[19:16] Select (AC11, AD11, AE11, AF11)
- 0 SA[19:16]... default
- 1 GPO[19:16]

4 GPIO[15:12] Direction
- 0 Input (pins are GPI[15:12]) .... default
- 1 Output (pins are GPO[15:12])

3 GPIO[11:8] Direction
- 0 Input (pins are GPI[11:8]) .... default
- 1 Output (pins are GPO[11:8])

2 GNT5# / GPO7 Select (Pin P4)
REQ5# / GPI7 Select (Pin N4)
- 0 P4 = GPO7, N4 = GPI7........................ default
- 1 P4 = GNT5#, N4 = REQ5#

1 PCISTP# / GPO6 Select (Pin AF6)
- 0 V6 = PCISTP#....................................... default
- 1 V6 = GPO6

0 CPUSTP# / GPO5 Select (Pin AC7)
- 0 Y5 = CPUSTP#..................................... default
- 1 Y5 = GPO5

Offset E5 – GPIO I/O Select 1 .... RW

7 Voltage Regulator Change Timer Select
- 0 100 usec .... default
- 1 200 usec

6 AGPBZ# Source of Bus Master Status
- 0 Disable .... default
- 1 Enable

5 Reserved ....always reads 0

4 VGATE on GPIO8 (Pin C8)
- 0 U2 = GPIO8.. default
- 1 U2 = VGATE (bit 1 and RxE4[6] are ignored)

3 CPU Frequency Change
- 0 Enable .... default
- 1 Disable

2 PCS1# on ACSDIN3 (Pin V1)
- 0 V1 = ACSDIN3 / GPIO21 / SLPBTN#. default
- 1 V1 = PCS1# (RxE4[6] ignored)

1 PCS0# on ACSDIN2 (Pin U2)
- 0 U2 = ACSDIN2 / GPIO20.................... default
- 1 U2 = PCS0# (RxE4[6] ignored)

0 IORDY / GPI19 Select (Pin AD10)
- 0 AD10 = IORDY.................................... default
- 1 AD10 = GPI19

Offset E6 – GPIO I/O Select 2 .... RW

7 GPI31 / GPO31 (GPIOE) Select (Pin AC6)
- 0 AC6 = GPI31.. default
- 1 AC6 = GPO31 / GPIOE

6 GPI30 / GPO30 (GPIOD) Select (Pin AD6)
- 0 AD6 = GPI30.. default
- 1 AD6 = GPO30 / GPIOD

5-2 Reserved ....always reads 0

1 GPI25 / GPO25 (GPIOC) Select (Pin AE6)
- 0 AE6 = GPI25 .... default
- 1 AE6 = GPO25 / GPIOC

0 GPI24 / GPO24 (GPIOA) Select (Pin AE5)
- 0 AE5 = GPI24 .... default
- 1 AE5 = GPO24 / GPIOA

Offset E7 – GPO Output Type.. RW

These bits determine whether the indicated GPO pin is open drain or TTL when the corresponding bit of RxE6 = 1.

7 GPO31 OD/TTL Select (Pin AC6)
6 GPO30 OD/TTL Select (Pin AD6)
5-2 Reserved ....always reads 0
1 GPO25 OD/TTL Select (Pin AE6)
0 GPO24 OD/TTL Select (Pin AE5)

For all defined bits above:
- 0 OD .... default
- 1 TTL

Power Management I/O-Space Registers

Basic Power Management Control and Status

I/O Offset 1-0 - Power Management Status ....RWC

The bits in this register are set only by hardware and can be reset by software by writing a one to the desired bit position.

- **15 Wakeup Status** .... default = 0
  This bit is set when the system is in the suspend state and an enabled resume event occurs. Upon setting this bit, the system automatically transitions from the suspend state to the normal working state (from C3 to C0 for the processor).
- **14-12 Reserved** .... always reads 0
- **11 Abnormal Power-Off Status** .... default = 0
- **10 RTC Alarm Status** .... default = 0
  This bit is set when the RTC generates an alarm (on assertion of the RTC IRQ signal).
- **9 Sleep Button Status** .... default = 0
  This bit is set when the sleep button is pressed (SLPBTN# signal asserted low).
- **8 Power Button Status** .... default = 0
  This bit is set when the PWRBTN# signal is asserted low. If the PWRBTN# signal is held low for more than four seconds, this bit is cleared, the Power Button Status bit is set, and the system will transition into the soft off state.
- **7-6 Reserved** .... always reads 0
- **5 Global Status** .... default = 0
  This bit is set by hardware when the BIOS Release bit is set (typically by an SMI routine to release control of the SCI / SMI lock). When this bit is cleared by software (by writing a one to this bit position) the BIOS Release bit is also cleared at the same time by hardware.
- **4 Bus Master Status** .... default = 0
  This bit is set when a system bus master requests the system bus. All PCI master, ISA master and ISA DMA devices are included.
- **3-1 Reserved** .... always reads 0
- **0 ACPI Timer Carry Status** .... default = 0
  The bit is set when the 23rd (31st) bit of the 24 (32) bit ACPI power management timer changes.

I/O Offset 3-2 - Power Management Enable .... RW

The bits in this register correspond to the bits in the Power Management Status Register at offset 1-0.

- **15 Reserved** ....always reads 0
- **14-12 Reserved** ....always reads 0
- **11 Reserved** ....always reads 0
- **10 RTC Alarm Enable** ....default = 0
  This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI Enable bit) to be generated when the RTC Status bit is set.
- **9 Sleep Button Enable** ....default = 0
  This bit may be set to trigger either an SCI or SMI when the Sleep Button Status bit is set.
- **8 Power Button Enable** ....default = 0
  This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI Enable bit) to be generated when the Power Button Status bit is set.
- **7-6 Reserved** ....always reads 0
- **5 Global Enable** ....default = 0
  This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI Enable bit) to be generated when the Global Status bit is set.
- **4 Reserved** ....always reads 0
- **3-1 Reserved** ....always reads 0
- **0 ACPI Timer Enable**.................................default = 0
  This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI Enable bit) to be generated when the Timer Status bit is set.

I/O Offset 5-4 - Power Management Control..................RW

15 Soft Resume
This bit is used to allow a system using an AT power supply to operate as if an ATX power supply were being used. Refer to the BIOS Porting Guide for implementation details.
- 0 Disable .... default
- 1 Enable

14 Reserved .... always reads 0

13 Sleep Enable .... Write 1 to activate
This is a write-only bit; reads from this bit always return zero. Writing a one to this bit causes the system to sequence into the sleep (suspend) state defined by the Sleep Type field.

12-10 Sleep Type
- 000 Normal On
- 001 Suspend to RAM (STR)
- 010 Suspend to Disk (STD) (also called Soft Off). The VCC power plane is turned off while the VSUS33 and VBAT planes remain on.
- 011 Reserved
- 100 Power On Suspend without Reset
- 101 Power On Suspend with CPU Reset
- 110 Power On Suspend with CPU/PCI Reset
- 111 Reserved

In any sleep state, there is minimal interface between powered and non-powered planes so that the effort for hardware design may be well managed.

9 Reserved .... always reads 0

8 STD Command Generates System Reset Only
- 0 Disable .... default
- 1 Enable (STD command generates a system reset and not STD)

7-3 Reserved .... always reads 0

2 Global Release .... **WO**, default = 0
This bit is set by ACPI software to indicate the release of the SCI / SMI lock. Upon setting of this bit, the hardware automatically sets the BIOS Status bit. The bit is cleared by hardware when the BIOS Status bit is cleared by software. Note that the setting of this bit will cause an SMI to be generated if the BIOS Enable bit is set (bit-5 of the Global Enable register at offset 2Ah).

1 Bus Master Reload
This bit controls whether bus master requests (PMIO Rx00[4] = 1) transition the processor from C3 to C0 state.
- 0 Bus master requests are ignored by power management logic .... default
- 1 Bus master requests transition the processor from the C3 state to the C0 state

0 SCI / SMI Select
This bit controls whether SCI or SMI is generated for power management events triggered by the Power Button, Sleep Button, and RTC (when PMIO Rx1-0 bits 8, 9, or 10 equal one).
- 0 Generate SMI....................................... default
- 1 Generate SCI

Note that certain power management events can be programmed individually to generate an SCI or SMI independent of the setting of this bit (refer to the General Purpose SCI Enable and General Purpose SMI Enable registers at offsets 22 and 24). Also, Timer Status & Global Status always generate SCI and BIOS Status always generates SMI.

I/O Offset 0B-08 - Power Management Timer .... RW

31-24 Extended Timer Value
This field reads back 0 if the 24-bit timer option is selected (Rx41 bit-3).

23-0 Timer Value
This read-only field returns the running count of the power management timer. This is a 24/32-bit counter that runs off a 3.579545 MHz clock, and counts while in the S0 (working) system state. The timer is reset to an initial value of zero during a reset, and then continues counting until the 14.31818 MHz input to the chip is stopped. If the clock is restarted without a reset, then the counter will continue counting from where it stopped.

Processor Power Management Registers

I/O Offset 13-10 - Processor & PCI Bus Control............RW

31-12 Reserved .... always reads 0

11 Disable PCISTP# When PCKRUN# is Deasserted
- 0 Enable.. default
- 1 Disable

10 PCI Bus Clock Run Without Stop
- 0 PCKRUN# is always asserted .... default
- 1 PCKRUN# will be de-activated after the PCI bus is idle for 26 clocks

9 Host Clock Stop
This bit controls whether CPUSTP# is asserted in C3 and S1 states. Normally CPUSTP# is not asserted in C3 and S1 states, only STPCLK# is asserted.
- 0 CPUSTP# will not be asserted in C3 and S1 states (only STPCLK# is asserted)........ default
- 1 CPUSTP# will be asserted in C3 and S1 states

8 Assert SLP# for Processor Level 3 Read
This bit controls whether SLP# is asserted in C3 state.
- 0 SLP# is not asserted in C3 state .... default
- 1 SLP# is asserted in C3 state

Used with Intel CPUs only.

7 Lower CPU Voltage During C3 / S1
This bit controls whether the CPU voltage is lowered when in C3/S1 state. The voltage is lowered using the VRDSLP signal to the voltage regulator. PMIO RxE5[3] must be 0 to enable the voltage change function. Bits 8 and 9 of this register must also be set to 1.
- 0 Disable (normal voltage during C3/S1)....... def
- 1 Enable (lower voltage during C3/S1)

6-5 Reserved .... always reads 0

4 Throttling Enable
Setting this bit starts clock throttling (modulating the STPCLK# signal) regardless of the CPU state. The throttling duty cycle is determined by bits 3-0 of this register.

3-0 Throttling Duty Cycle
This field determines the duty cycle of the STPCLK# signal when the system is in throttling mode ("Throttling Enable" bit set to one). The duty cycle indicates the percentage of performance (the lower the percentage, the lower the performance and the higher the power savings).

0000 Reserved
0001 0-6.25%
0010 6.25-12.50%
0011 18.75-25.00%
0100 31.25-37.50%
0101 37.50-43.75%
0110 43.75-50.00%
0111 50.00-56.25%
1000 56.25-62.50%
1001 62.50-68.75%
1010 68.75-75.00%
1011 75.00-87.50%
1100 75.00-81.25%
1101 81.25-87.50%
1110 87.50-93.75%
1111 93.75-100%

I/O Offset 14 - Processor Level 2 .... RO

7-0 Level 2 .... always reads 0
Reads from this register put the processor into the Stop Grant state (the VT8235 asserts STPCLK# to suspend the processor). Wake up from Stop Grant state is by interrupt (INTR, SMI, and SCI).

Reads from this register return all zeros; writes to this register have no effect.

I/O Offset 15 - Processor Level 3 .... RO

7-0 Level 3 .... always reads 0
Reads from this register put the processor in the C3 clock state with the STPCLK# signal asserted. If Rx10[9] = 1 then the CPU clock is also stopped by asserting CPUSTP#. Wakeup from the C3 state is by interrupt (INTR, SMI, and SCI).

Reads from this register return all zeros; writes to this register have no effect.

General Purpose Power Management Registers

I/O Offset 21-20 - General Purpose Status ....RWC

- **15 North Bridge SERR# Status**
- **14 USB Wake-Up Status**
  For STR / STD / Soff
- **13 AC97 Wake-Up Status**
  Can be set only in suspend mode
- **12 Battery Low Status**
  Set when the BATLOW# input is asserted low.
- **11 Notebook Lid Status**
  Set when the LID input detects the edge selected by Rx2C bit-7 (0=rising, 1=falling).
- **10 Thermal Detect Status**
  Set when the THRM# input detects the edge selected by Rx2C bit-6 (0=rising, 1=falling).
- **9 Reserved** .... always reads 0
- **8 Ring Status**
  Set when the RING# input is asserted low.
- **7 Reserved** .... always reads 0
- **6 INTRUDER# Status**
  Set when the INTRUDER# pin is asserted low.
- **5 PME# Status**
  Set when the PME# pin is asserted low.
- **4 EXTSMI# Status**
  Set when the EXTSMI# pin is asserted low.
- **3 Internal LAN PME Status**
  Set when the internal LAN PME signal is asserted.
- **2 Internal KBC PME Status**
  Set when the internal KBC PME signal is asserted.
- **1 GPI1 Status**
  Set when the GPI1 pin is asserted low.
- **0 GPI0 Status**
  Set when the GPI0 pin is asserted low.

Note that the above bits correspond one for one with the bits of the General Purpose SCI Enable and General Purpose SMI Enable registers at offsets 22 and 24: an SCI or SMI is generated if the corresponding bit of the General Purpose SCI or SMI Enable registers, respectively, is set to one.

The above bits are set by hardware only and can only be cleared by writing a one to the desired bit.

I/O Offset 23-22 - General Purpose SCI Enable .... RW

- **15 Enable SCI on setting of Rx21-20[15]**.............def=0
- **14 Enable SCI on setting of Rx21-20[14]**.............def=0
- **13 Enable SCI on setting of Rx21-20[13]**.............def=0
- **12 Enable SCI on setting of Rx21-20[12]**.............def=0
- **11 Enable SCI on setting of Rx21-20[11]**.............def=0
- **10 Enable SCI on setting of Rx21-20[10]**.............def=0
- **9 Reserved** .... always reads 0
- **8 Enable SCI on setting of Rx21-20[8]**...............def=0
- **7 Reserved** .... always reads 0
- **6 Enable SCI on setting of Rx21-20[6]**...............def=0
- **5 Enable SCI on setting of Rx21-20[5]**...............def=0
- **4 Enable SCI on setting of Rx21-20[4]**...............def=0
- **3 Enable SCI on setting of Rx21-20[3]**...............def=0
- **2 Enable SCI on setting of Rx21-20[2]**...............def=0
- **1 Enable SCI on setting of Rx21-20[1]**...............def=0
- **0 Enable SCI on setting of Rx21-20[0]**...............def=0

These bits allow generation of an SCI using a separate set of conditions from those used for generating an SMI.

I/O Offset 25-24 - General Purpose SMI Enable .... RW

- **15 Enable SMI on setting of Rx21-20[15]**............def=0
- **14 Enable SMI on setting of Rx21-20[14]**............def=0
- **13 Enable SMI on setting of Rx21-20[13]**............def=0
- **12 Enable SMI on setting of Rx21-20[12]**............def=0
- **11 Enable SMI on setting of Rx21-20[11]**............def=0
- **10 Enable SMI on setting of Rx21-20[10]**............def=0
- **9 Reserved** .... always reads 0
- **8 Enable SMI on setting of Rx21-20[8]**..............def=0
- **7 Reserved** .... always reads 0
- **6 Enable SMI on setting of Rx21-20[6]**..............def=0
- **5 Enable SMI on setting of Rx21-20[5]**..............def=0
- **4 Enable SMI on setting of Rx21-20[4]**..............def=0
- **3 Enable SMI on setting of Rx21-20[3]**..............def=0
- **2 Enable SMI on setting of Rx21-20[2]**..............def=0
- **1 Enable SMI on setting of Rx21-20[1]**..............def=0
- **0 Enable SMI on setting of Rx21-20[0]**..............def=0

These bits allow generation of an SMI using a separate set of conditions from those used for generating an SCI.

Generic Power Management Registers

I/O Offset 29-28 - Global Status ....RWC

- **15 GPIO Range 1 Access Status**.................. default = 0
- **14 GPIO Range 0 Access Status**.................. default = 0
- **13 GP3 Timer Timeout Status** .... default = 0
- **12 GP2 Timer Timeout Status** .... default = 0
- **11 SERIRQ SMI Status**............................... default = 0
- **10 Rx5[5] Write SMI Status**........................ default = 0
  This bit reports whether Rx5[5] is written. If Rx2B[3] is set to enable SMI, an SMI in generated when this bit = 1.
- **9 Reserved** .... always reads 0
- **8 PCKRUN# Resume Status** .... default = 0
  This bit is set when PCI bus peripherals wake up the system by asserting PCKRUN#
- **7 Primary IRQ/INIT/NMI/SMI Resume Status**def=0
  This bit is set at the occurrence of primary IRQs as defined in Rx85-84 of PCI configuration space
- **6 Software SMI Status**............................... default = 0
  This bit is set when the SMI Command port (Rx2F) is written.
- **5 BIOS Status**... default = 0
  This bit is set when the Global Release bit is set to one (typically by the ACPI software to release control of the SCI/SMI lock). When this bit is reset (by writing a one to this bit position) the Global Release bit is reset at the same time by hardware.
- **4 Legacy USB Status**.................................. default = 0
  This bit is set when a legacy USB event occurs. This is normally used for USB keyboards.
- **3 GP1 Timer Time Out Status** .... default = 0
  This bit is set when the GP1 timer times out.
- **2 GP0 Timer Time Out Status** .... default = 0
  This bit is set when the GP0 timer times out.
- **1 Secondary Event Timer Time Out Status**...... def=0
  This bit is set when the secondary event timer times out.
- **0 Primary Activity Status**........................... default = 0
  This bit is set at the occurrence of any enabled primary system activity (see the Primary Activity Detect Status register at offset 30h and the Primary Activity Detect Enable register at offset 34h). After checking this bit, software can check the status bits in the Primary Activity Detect Status register at offset 30h to identify the specific source of the primary event. Note that setting this bit can be enabled to reload the GP0 timer (see bit-0 of the GP Timer Reload Enable register at offset 38).

Note that SMI can be generated based on the setting of any of the above bits (see the Rx2A Global Enable register bit descriptions in the right hand column of this page).

The bits in this register are set by hardware only and can only be cleared by writing a one to the desired bit position.

The bits in this register are for SMI's only while the bits in Rx21-20 are for SMI's and SCI's

I/O Offset 2B-2A - Global Enable .... RW

- **15 GPIO Range 1 SMI Enable** ....default = 0
- **14 GPIO Range 0 SMI Enable** ....default = 0
- **13 GP3 Timer Timeout SMI Enable**...........default = 0
- **12 GP2 Timer Timeout SMI Enable**...........default = 0
- **11 SERIRQ SMI Enable**...............................default = 0
- **10 SMI on Sleep Enable Write** ....default = 0
- **9 Reserved** ....always reads 0
- **8 PCKRUN# Resume Enable** ....default = 0
  This bit may be set to trigger an SMI to be generated when the PCKRUN# Resume Status bit is set.
- **7 Primary IRQ/INIT/NMI/SMI Resume Enable In Post State** ....default = 0
  This bit may be set to trigger an SMI to be generated when the Primary IRQ / INIT / NMI / SMI Resume Status bit is set.
- **6 SMI on Software SMI** ....default = 0
  This bit may be set to trigger an SMI to be generated when the Software SMI Status bit is set.
- **5 SMI on BIOS Status**................................default = 0
  This bit may be set to trigger an SMI to be generated when the BIOS Status bit is set.
- **4 SMI on Legacy USB** ....default = 0
  This bit may be set to trigger an SMI to be generated when the Legacy USB Status bit is set.
- **3 SMI on GP1 Timer Time Out**.................default = 0
  This bit may be set to trigger an SMI to be generated when the GP1 Timer Timeout Status bit is set.
- **2 SMI on GP0 Timer Time Out**.................default = 0
  This bit may be set to trigger an SMI to be generated when the GP0 Timer Timeout Status bit is set.
- **1 SMI on Secondary Event Timer Time Out** ....def=0
  This bit may be set to trigger an SMI to be generated when the Secondary Event Timer Timeout Status bit is set.
- **0 SMI on Primary Activity** ....default = 0
  This bit may be set to trigger an SMI to be generated when the Primary Activity Status bit is set.

I/O Offset 2D-2C - Global Control..................................RW

15-12 Reserved .... always reads 0

11 IDE Secondary Bus Power-Off
- 0 Disable .... default
- 1 Enable

10 IDE Primary Bus Power-Off
- 0 Disable .... default
- 1 Enable

9 Reserved .... always reads 0

8 SMI Active
- 0 SMI Inactive.. default
- 1 SMI Active. If the SMI Lock bit is set, this bit needs to be written with a 1 to clear it before the next SMI can be generated.

7 LID Triggering Polarity
- 0 Rising Edge .... default
- 1 Falling Edge

6 THRM# Triggering Polarity
- 0 Rising Edge .... default
- 1 Falling Edge

5 Battery Low Resume Disable
- 0 Enable resume .... default
- 1 Disable resume from suspend when BATLOW# is asserted

4-3 Reserved .... always reads 0

2 Power Button Triggering Select
- 0 SCI/SMI generated by PWRBTN# rising edge .... default
- 1 SCI/SMI generated by PWRBTN# falling edge

Set to zero to avoid the situation where the Power Button Status bit is set to wake up the system then reset again by PBOR Status to switch the system into the soft-off state.

1 BIOS Release

This bit is set by legacy software to indicate release of the SCI/SMI lock. Upon setting of this bit, hardware automatically sets the Global Status bit. This bit is cleared by hardware when the Global Status bit cleared by software.

Note that if the Global Enable bit is set (Power Management Enable register Rx2[5]), then setting this bit causes an SCI to be generated (because setting this bit causes the Global Status bit to be set).

0 SMI Enable
- 0 Disable all SMI generation.................... default
- 1 Enable SMI generation

I/O Offset 2F - SMI Command..RW

7-0 SMI Command

Writing to this port sets the Software SMI Status bit. Note that if the Software SMI Enable bit is set (see Global Enable register Rx2A[6]), then an SMI is generated.

I/O Offset 33-30 - Primary Activity Detect Status.......RWC

These bits correspond to the Primary Activity Detect Enable bits in Rx37-34. If the corresponding bit is set in that register, setting of a bit below will cause the Primary Activity Status (PACT_STS) bit to be set (Global Status register Rx28[0]). All bits in this register default to 0, are set by hardware only, and may only be cleared by writing 1s to the desired bit.

31-11 Reserved ....always read 0

10 Audio Access Status .... (AUD_STS)
Set if Audio is accessed.

9 Keyboard Controller Access Status..... (KBC_STS)
Set if the KBC is accessed via I/O port 60h.

8 VGA Access Status................................(VGA_STS)
Set if the VGA port is accessed via I/O ports 3B0-3DFh or memory space A0000-BFFFFh.

7 Parallel Port Access Status.................... (LPT_STS)
Set if the parallel port is accessed via I/O ports 278-27Fh or 378-37Fh (LPT2 or LPT1).

6 Serial Port B Access Status .... (COMB_STS)
Set if the serial port is accessed via I/O ports 2F8-2FFh or 2E8-2Efh (COM2 and COM4 respectively).

5 Serial Port A Access Status .... (COMA_STS)
Set if the serial port is accessed via I/O ports 3F8-3FFh or 3E8-3EFh (COM1 and COM3, respectively).

4 Floppy Access Status..............................(FDC_STS)
Set if the floppy controller is accessed via I/O ports 3F0-3F5h or 3F7h.

3 Secondary IDE Access Status...............(SIDE_STS)
Set if the IDE controller is accessed via I/O ports 170-177h or 376h.

2 Primary IDE Access Status .... (PIDE_STS)
Set if the IDE controller is accessed via I/O ports 1F0-1F7h or 3F6h.

1 Primary Interrupt Activity Status...... (PIRQ_STS)
Set on the occurrence of a primary interrupt (enabled via the "Primary Interrupt Channel" register at Function 4 PCI configuration register offset 44h).

0 PCI Master Access Status..................... (DRQ_STS)
Set on the occurrence of PCI master activity.

Note: Setting of Primary Activity Status (PACT_STS) may be done to enable a "Primary Activity Event": an SMI will be generated if the Primary Activity Enable bit is set (Global Enable register Rx2A[0]) and/or the GP0 timer will be reloaded if the "GP0 Timer Reload on Primary Activity" bit is set (GP Timer Reload Enable register Rx38[0]).

Note: Bits 2-9 above also correspond to bits of GP Timer Reload Enable register Rx38: If bits are set in that register, setting a corresponding bit in this register will cause the GP1 timer to be reloaded.

I/O Offset 37-34 - Primary Activity Detect Enable........ RW

These bits correspond to the Primary Activity Detect Status bits in Rx33-30. Setting of any of these bits also sets the Primary Activity Status (PACT_STS) bit (Rx28[0]) which causes the GP0 timer to be reloaded (if the Primary Activity GP0 Enable bit is set) or generates an SMI (if Primary Activity Enable is set).

31-11 Reserved .... always read 0

10 SMI on Audio Status .... (AUD_EN)
- 0 Don't set PACT_STS if AUD_STS is set .... def
- 1 Set PACT_STS if AUD_STS is set

9 SMI on Keyboard Controller Status..... (KBC_EN)
- 0 Don't set PACT_STS if KBC_STS is set..... def
- 1 Set PACT_STS if KBC_STS is set

8 SMI on VGA Status................................ (VGA_EN)
- 0 Don't set PACT_STS if VGA_STS is set .... def
- 1 Set PACT_STS if VGA_STS is set

7 SMI on Parallel Port Status.................... (LPT_EN)
- 0 Don't set PACT_STS if LPT_STS is set...... def
- 1 Set PACT_STS if LPT_STS is set

6 SMI on Serial Port B Status .... (COMB_EN)
- 0 Don't set PACT_STS if COMB_STS is set . def
- 1 Set PACT_STS if COMB_STS is set

5 SMI on Serial Port A Status .... (COMA_EN)
- 0 Don't set PACT_STS if COMA_STS is set . def
- 1 Set PACT_STS if COMA_STS is set

4 SMI on Floppy Status..............................(FDC_EN)
- 0 Don't set PACT_STS if FDC_STS is set ..... def
- 1 Set PACT_STS if FDC_STS is set

3 SMI on Secondary IDE Status...............(SIDE_EN)
- 0 Don't set PACT_STS if SIDE_STS is set .... def
- 1 Set PACT_STS if SIDE_STS is set

2 SMI on PrimaryIDE Status .... (PIDE_EN)
- 0 Don't set PACT_STS if PIDE_STS is set .... def
- 1 Set PACT_STS if PIDE_STS is set

1 SMI on Primary IRQ Status................. (PIRQ_EN)
- 0 Don't set PACT_STS if PIRQ_STS is set.... def
- 1 Set PACT_STS if PIRQ_STS is set

0 SMI on PCI Master Status..................... (DRQ_EN)
- 0 Don't set PACT_STS if DRQ_STS is set .... def
- 1 Set PACT_STS if DRQ_STS is set

I/O Offset 3B-38 - GP Timer Reload Enable ....RW

All bits in this register default to 0 on power up.

31-8 Reserved .... always reads 0

7 GP1 Timer Reload on KBC Access
- 0 Normal GP1 Timer Operation............... default
- 1 Setting of KBC_STS causes the GP1 timer to reload.

6 GP1 Timer Reload on Serial Port Access
- 0 Normal GP1 Timer Operation .... default
- 1 Setting of COMA_STS or COMB_STS causes the GP1 timer to reload.

5 Reserved .... always reads 0

4 GP1 Timer Reload on VGA Access
- 0 Normal GP1 Timer Operation .... default
- 1 Setting of VGA_STS causes the GP1 timer to reload.

3 GP1 Timer Reload on IDE/Floppy Access
- 0 Normal GP1 Timer Operation .... default
- 1 Setting of FDC_STS, SIDE_STS, or PIDE_STS causes the GP1 timer to reload.

2 GP3 Timer Reload on GPIO Range 1 Access
- 0 Normal GP3 Timer Operation .... default
- 1 Setting of GR1_STS causes the GP3 timer to reload.

1 GP2 Timer Reload on GPIO Range 0 Access
- 0 Normal GP2 Timer Operation .... default
- 1 Setting of GR0_STS causes the GP2 timer to reload.

0 GP0 Timer Reload on Primary Activity
- 0 Normal GP0 Timer Operation .... default
- 1 Setting of PACT_STS causes the GP0 timer to reload. Primary activities are enabled via the Primary Activity Detect Enable register (offset 37-34) with status recorded in the Primary Activity Detect Status register (offset 33-30).

I/O Offset 40 – Extended I/O Trap Status .... RWC

7-5 Reserved .... always reads 0

4 BIOS Write Access Status

3 GP3 Timer Second Timeout With No Cycles
- 0 Disable .... default
- 1 Enable (GP3 timer timed out twice with no cycles in between)

2 GP3 Timer Second Timeout Status

1 GPIO Range 3 Access Status

0 GPIO Range 2 Access Status

I/O Offset 42 – Extended I/O Trap Enable..................... RW

7-5 Reserved .... always reads 0

4 SMI on BIOS Write Access

This bit controls whether SMI is generated when BIOS Write Access Status Rx40[4] = 1.
- 0 Disable .... default
- 1 Enable (can be reset only by OCI_Reset)

3 Reserved .... always reads 0

2 GP3 Timer Second Timeout Reboot

This bit controls whether the system is rebooted when the GP3 timer times out twice (Rx40[2] = 1).
- 0 Disable .... default
- 1 Enable

1 SMI on GPIO Range 3 Access

This bit controls whether SMI is generated when GPIO range 3 is accessed (Rx40[1] = 1)
- 0 Disable .... default
- 1 Enable

0 SMI on GPIO Range 2 Access

This bit controls whether SMI is generated when GPIO range 2 is accessed (Rx40[0] = 1)
- 0 Disable .... default
- 1 Enable

General Purpose I/O Registers

I/O Offset 45 – SMI / IRQ / Resume Status .... RO

- **7-5 Reserved** .... always reads 0
- **4 Latest PCSn Status**
  - 0 Latest PCSn was an I/O Read
  - 1 Latest PCSn was an I/O Write
- **3 Serial SMI Status**
  This bit is used to report a Serial-IRQ-generated SMI.
- **2 Reserved** .... always reads 0
- **1 SMBus IRQ Status**
  This bit is used to report an SMBus SMI.
- **0 SMBus Resume Status**
  This bit is used to report an SMBus Resume Event.

I/O Offset 4B-48 - GPI Port Input Value (GPIVAL) ..... RO

- **31-0 GPI[31-0] Input Value** .... Read Only

I/O Offset 4F-4C - GPO Port Output Value (GPOVAL)RW

Reads from this register return the last value written (held on chip). Some GPIO pins can be used as both input and output (GPIO pins 8-15 and 20-31). The output type of these pins is OD (open drain) so to use one of these pins as an input pin, a one must be written to the corresponding bit of this register. See also Function 0 RxE4[4-3] for I/O control of GPIO pins 8-15.

- **31-0 GPO[31-0] Output Value**.............def = FFFFFFFFh

I/O Offset 50 – GPI Pin Change Status ....RW

- **7 GPI27 Pin Change Status** .... default = 0
- **6 GPI26 Pin Change Status** .... default = 0
- **5 GPI25 Pin Change Status** .... default = 0
- **4 GPI24 Pin Change Status** .... default = 0
- **3 GPI19 Pin Change Status** .... default = 0
- **2 GPI18 Pin Change Status** .... default = 0
- **1 GPI17 Pin Change Status** .... default = 0
- **0 GPI16 Pin Change Status** .... default = 0

I/O Offset 52 – GPI Pin Change SCI/SMI Select............RW

- **7 GPI27 Pin SCI / SMI Select**
- **6 GPI26 Pin SCI / SMI Select**
- **5 GPI25 Pin SCI / SMI Select**
- **4 GPI24 Pin SCI / SMI Select**
- **3 GPI19 Pin SCI / SMI Select**
- **2 GPI18 Pin SCI / SMI Select**
- **1 GPI17 Pin SCI / SMI Select**
- **0 GPI16 Pin SCI / SMI Select**
  - 0 SCI on pin input change .... default
  - 1 SMI on pin input change

I/O Trap Registers

I/O Offset 57-54 – I/O Trap PCI Data ....RO

- **31-0 PCI Data During I/O Trap SMI**

I/O Offset 59-58 – I/O Trap PCI I/O Address.................RO

- **15-0 PCI Address During I/O Trap SMI**

I/O Offset 5A – I/O Trap PCI Command / Byte Enable RO

- **7-4 PCI Command Type During I/O Trap SMI**
- **3-0 PCI Byte Enable During I/O Trap SMI**

I/O Offset 5C – CPU Performance Control.................... RW

- **7-2 Reserved** ....always reads 0
- **1 Lower CPU Voltage During C3 / S1**
  This bit controls the CPU voltage in C3/S1 state. The voltage is lowered using the VGATE signal (PMIO RxE5[4] must be 0 to enable the voltage change function).
  - 0 Disable (normal voltage during C3/S1) ....def
  - 1 Enable (lower voltage during C3/S1)
- **0 Lower CPU Frequency During C3 / S1**
  This bit controls the CPU frequency in C3/S1 state. The frequency is lowered using the GHI# signal (PMIO RxE5[3] must be 0 to enable the frequency change function).
  - 0 Disable (normal frequency during C3/S1)...def
  - 1 Enable (lower frequency during C3/S1)

System Management Bus I/O-Space Registers

The base address for these registers is defined in RxD1-D0 of the Device 17 Function 0 PCI configuration registers. The System Management Bus I/O space is enabled for access by the system if Device 17 Function 0 RxD2[0] = 1.

I/O Offset 00 – SMBus Host Status..............................RWC

- **7 Reserved** .... always reads 0
- **6 SMB Semaphore..RWC**
  This bit is used as a semaphore among various independent software threads that may need to use the Host SMBus logic and has no effect on hardware. After reset, this bit reads 0. Writing 1 to this bit causes the next read to return 0, then all reads after that return 1. Writing 0 to this bit has no effect. Software can therefore write 1 to request control and if readback is 0 then it will own usage of the host controller.
- **5 Reserved** .... always reads 0
- **4 Failed Bus Transaction....................................RWC**
  - 0 SMBus interrupt not caused by failed bus transaction .... default
  - 1 SMBus interrupt caused by failed bus transaction. This bit may be set when the KILL bit (I/O Rx02[1]) is set and can be cleared by writing a 1 to this bit position.
- **3 Bus Collision...RWC**
  - 0 SMBus interrupt not caused by transaction collision .... default
  - 1 SMBus interrupt caused by transaction collision. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
- **2 Device Error ....RWC**
  - 0 SMBus interrupt not caused by generation of an SMBus transaction error.................. default
  - 1 SMBus interrupt caused by generation of an SMBus transaction error (illegal command field, unclaimed host-initiated cycle, or host device timeout). This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
- **1 SMBus Interrupt...RWC**
  - 0 SMBus interrupt not caused by host command completion.. default
  - 1 SMBus interrupt caused by host command completion. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
- **0 Host Busy .... RO**
  - 0 SMBus controller host interface is not processing a command .... default
  - 1 SMBus host controller is busy processing a command. None of the other SMBus registers should be accessed if this bit is set.

I/O Offset 01h – SMBus Slave Status.......................... RWC

- **7-6 Reserved** ....always reads 0
- **5 Alert Status .... RWC**
  - 0 SMBus interrupt not caused by SMBALERT# signal .... default
  - 1 SMBus interrupt caused by SMBALERT# signal. This bit will be set only if the Alert Enable bit is set in the SMBus Slave Control Register at I/O Offset R08[3]. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
- **4 Shadow 2 Status.. RWC**
  - 0 SMBus interrupt not caused by address match to SMBus Shadow Address Port 2......... default
  - 1 SMBus interrupt or resume event caused by slave cycle address match to SMBus Shadow Address Port 2. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
- **3 Shadow 1 Status.. RWC**
  - 0 SMBus interrupt not caused by address match to SMBus Shadow Address Port 1......... default
  - 1 SMBus interrupt or resume event caused by slave cycle address match to SMBus Shadow Address Port 1. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
- **2 Slave Status .... RWC**
  - 0 SMBus interrupt not caused by slave event match .... default
  - 1 SMBus interrupt or resume event caused by slave cycle event match of the SMBus Slave Command Register at PCI Function 4 Configuration Offset D3h (command match) and the SMBus Slave Event Register at SMBus Base + Offset 0Ah (data event match). This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
- **1 Reserved** ....always reads 0
- **0 Slave Busy .... RO**
  - 0 SMBus controller slave interface is not processing data .... default
  - 1 SMBus controller slave interface is busy receiving data. None of the other SMBus registers should be accessed if this bit is set.

I/O Offset 02h – SMBus Host Control............................RW

7 Reserved .... always reads 0

6 Start .... always reads 0

- 0 Writing 0 has no effect .... default
- 1 Start Execution of Command
  Writing a 1 to this bit causes the SMBus controller host interface to initiate execution of the command programmed in the SMBus Command Protocol field (bits 4-2). All necessary registers should be programmed prior to writing a 1 to this bit. The Host Busy bit (SMBus Host Status Register bit-0) can be used to identify when the SMBus controller has completed command execution.

5-2 SMBus Command Protocol

Selects the type of command the SMBus host controller will execute. Reads or Writes are determined by Rx04[0].

- 0000 Quick default
- 0001 Byte
- 0010 Byte Data
- 0011 Word Data
- 0100 Process Call
- 0101 Block
- 0110 I2C with 10-bit Address
- 0111 -reserved-
- 10xx -reserved-
- 1100 I2C Process Call
- 1101 I2C Block
- 1110 I2C with 7-bit Address
- 1111 Universal

1 Kill Transaction in Progress

- 0 Normal host controller operation........... default
- 1 Stop host transaction currently in progress.
  Setting this bit also sets the FAILED status bit (Host Status bit-4) and asserts the interrupt selected by the SMB Interrupt Select bit (Function 4 SMBus Host Configuration Register RxD2[3]).

0 Interrupt Enable

- 0 Disable interrupt generation .... default
- 1 Enable generation of interrupts on completion of the current host transaction.

I/O Offset 03h – SMBus Host Command....................... RW

7-0 SMBUS Host Command ....default = 0

This field contains the data transmitted in the command field of the SMBus host transaction.

I/O Offset 04h – SMBus Host Address........................... RW

The contents of this register are transmitted in the address field of the SMBus host transaction.

7-1 SMBUS Address ....default = 0

This field contains the 7-bit address of the targeted slave device.

0 SMBUS Read or Write

- 0 Execute a WRITE command .... default
- 1 Execute a READ command

I/O Offset 05h – SMBus Host Data 0 .... RW

The contents of this register are transmitted in the Data 0 field of SMBus host transaction writes. On reads, Data 0 bytes are stored here.

7-0 SMBUS Data 0...default = 0

For Block Write commands, this field is programmed with the block transfer count (a value between 1 and 32). Counts of 0 or greater than 32 are undefined. For Block Read commands, the count received from the SMBus device is stored here.

I/O Offset 06h – SMBus Host Data 1 .... RW

The contents of this register are transmitted in the Data 1 field of SMBus host transaction writes. On reads, Data 1 bytes are stored here.

7-0 SMBUS Data 1...default = 0

I/O Offset 07h – SMBus Block Data............................... RW

Reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array. It is reset to 0 by reads of the SMBus Host Control register (I/O Offset 2) and incremented automatically by each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0.

7-0 SMBUS Block Data ....default = 0

I/O Offset 08h – SMBus Slave Control............................RW

7-5 Reserved .... always reads 0

4 SMBus GPIO Slave Enable

0 Disable .... default

1 Enable generation of a resume event upon an external SMBus master generating a transaction with an address that matches the GPIO Slave Address register (I/O offset 0Fh).

3 SMBus Alert Enable

0 Disable .... default

1 Enable generation of an interrupt or resume event on the assertion of the SMBALERT# signal

2 SMBus Shadow Port 2 Enable

0 Disable .... default

1 Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus Slave Shadow Port 2 register (PCI function 4 configuration register RxD5).

1 SMBus Shadow Port 1 Enable

0 Disable .... default

1 Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus Slave Shadow Port 1 register (PCI function 4 configuration register RxD4).

0 SMBus Slave Enable

0 Disable .... default

1 Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus host controller slave port of 10h, a command field which matches the SMBus Slave Command register (PCI function 4 configuration register RxD3), and a match of one of the corresponding enabled events in the SMBus Slave Event Register (I/O Offset 0Ah).

I/O Offset 09h – SMBus Shadow Command................... RO

This register is used to store command values for external SMBus master accesses to the host slave and slave shadow ports.

7-0 Shadow Command .... default = 0

This field contains the command value which was received during an external SMBus master access whose address field matched the host slave address (10h) or one of the slave shadow port addresses.

I/O Offset 0B-0Ah – SMBus Slave Event........................ RW

This register is used to enable generation of interrupt or resume events for accesses to the host controller's slave port.

15-0 SMBus Slave Event ....default = 0

This field contains data bits used to compare against incoming data to the SMBus Slave Data Register (I/O Offset 0Ch). When a bit in this register is set and the corresponding bit the Slave Data register is also set, an interrupt or resume event will be generated if the command value matches the value in the SMBus Slave Command register and the access was to SMBus host address 10h.

I/O Offset 0D-0Ch – SMBus Slave Data .... RO

This register is used to store data values for external SMBus master accesses to the shadow ports or the SMBus host controller's slave port.

15-0 SMBus Slave Data ....default = 0

This field contains the data value which was transmitted during an external SMBus master access whose address field matched one of the slave shadow port addresses or the SMBus host controller slave port address of 10h.

I/O Offset 0Fh – SMBus GPIO Slave Address (30h) ..... RW

7-1 SMBus GPIO Slave Address ....default = 0

This field specifies the address to match against incoming SMBus addresses for a GPIO slave.

0 Reserved ....always reads 0

Device 17 Function 1 Registers - Enhanced IDE Controller

This Enhanced IDE controller interface is fully compatible with the SFF 8038i v.1.0 specification. There are two sets of software accessible registers -- PCI configuration registers and Bus Master IDE I/O registers. The PCI configuration registers are located in the function 1 PCI configuration space of the VT8235. The Bus Master IDE I/O registers are defined in the SFF8038i v1.0 specification.

PCI Configuration Space Header

Offset 1-0 - Vendor ID (1106h=VIA) .... RO

Offset 3-2 - Device ID (0571h=IDE Controller) .... RO

Offset 5-4 – Command (0000h) ....RW

- **15-3 Reserved** .... always reads 0
- **2 Bus Master** .... default = 0 (disabled)
  S/G operation can be issued only when the "Bus Master" bit is enabled.
- **1 Reserved** .... always reads 0
- **0 I/O Space** .... default = 0 (disabled)
  When the "I/O Space" bit is disabled, the device will not respond to any I/O addresses for both compatible and native mode.

Offset 7-6 – Status (0290h)) .... RO

- **15 Detected Parity Error** .... fixed at 0
- **14 Signalled System Error** .... fixed at 0
- **13 Received Master Abort** .... default = 0
- **12 Received Target Abort** .... default = 0
- **11 Signalled Target Abort** .... fixed at 0
- **10-9 DEVSEL# Timing** .... **always reads 01** (medium)
- **8 Data Parity Detected** .... fixed at 0
- **7 Fast Back to Back** .... fixed at 1
- **6-5 Reserved** .... always reads 0
- **4 Capability List** .... fixed at 1
- **3-0 Reserved** .... always reads 0

Offset 8 - Revision ID (06) .... RO

- **7-0 Revision Code for IDE Controller Logic Block**

Offset 9 - Programming Interface .... RW

- **7 Master IDE Capability** .... fixed at 1 (Supported)
- **6-4 Reserved** .... always reads 0
- **3 Programmable Indicator - Secondary** ...... fixed at 1
  Supports both modes (may be set to either mode by writing Rx42[6])
- **2 Channel Operating Mode - Secondary**
  - 0 Compatibility Mode .... default
  - 1 Native Mode
- **1 Programmable Indicator - Primary** .... fixed at 1
  Supports both modes (may be set to either mode by writing Rx42[7])
- **0 Channel Operating Mode - Primary**
  - 0 Compatibility Mode .... default
  - 1 Native Mode

Compatibility Mode (fixed IRQs and I/O addresses):

Channel	Command Block Registers	Control Block Registers	IRQ
Pri	1F0-1F7	3F6	14
Sec	170-177	376	15

Native PCI Mode (registers are programmable in I/O space)

Channel	Command Block Registers	Control Block Registers
Pri	BA @offset 10h	BA @offset 14h
Sec	BA @offset 18h	BA @offset 1Ch

Command register blocks are 8 bytes of I/O space
Control registers are 4 bytes of I/O space (only byte 2 is used)

Offset A - Sub Class Code (01h=IDE Controller) .... RO

Offset B - Base Class Code (01h=Mass Storage Ctrlr) ... RO

Offset 13-10 - Pri Data / Command Base Address..........RW

Specifies an 8 byte I/O address space.

31-16	**Reserved**	always read 0
15-3	**Port Address**	default=01F0h
2-0	**Fixed at 001b**	fixed

Offset 17-14 - Pri Control / Status Base Address............RW

Specifies a 4 byte I/O address space of which only the third byte is active (i.e., 3F6h for the default base address of 3F4h).

31-16	**Reserved**	always read 0
15-2	**Port Address**	default=03F4h
1-0	**Fixed at 01b**	fixed

Offset 1B-18 - Sec Data / Command Base Address ....RW

Specifies an 8 byte I/O address space.

31-16	**Reserved**	always read 0
15-3	**Port Address**	default=0170h
2-0	**Fixed at 001b**	fixed

Offset 1F-1C - Sec Control / Status Base Address..........RW

Specifies a 4 byte I/O address space of which only the third byte is active (i.e., 376h for the default base address of 374h).

31-16	**Reserved**	always read 0
15-2	**Port Address**	default=0374h
1-0	**Fixed at 01b**	fixed

Offset 23-20 - Bus Master Control Regs Base Address ..RW

Specifies a 16 byte I/O address space compliant with the **SFF-8038**i **rev 1.0** specification.

31-16	**Reserved**	always read 0
15-4	**Port Address**	default=CC0h
3-0	**Fixed at 0001b**	fixed

See Rx42[7-6] for Native / Compatibility mode select for the above registers

Offset 2D-2C – Sub Vendor ID (0000h) .... RO

The readback value may be changed by writing to RxD5-D4.

Offset 2F-2E – Sub Device ID (0000h) .... RO

The readback value may be changed by writing to RxD7-D6.

Offset 34 - Capability Pointer (C0h) .... RO

Offset 3C - Interrupt Line (0Eh) .... RO

7-4 Reserved .... always read 0

3-0 IDE Interrupt Routing (for native mode)

0000 Disable
0001 IRQ1
0010 IRQ2
… …
1101 IRQ13
1110 IRQ14 .... default
1111 IRQ15
APIC (See Device 17 Function 0 Rx4D[7])
x000 IRQ16
x001 IRQ17
x010 IRQ18
… …
x111 IRQ23

Offset 3D - Interrupt Pin (00h).. RO

7-0 Interrupt Routing Mode

00h Legacy mode interrupt routing .... default
01h Native mode interrupt routing

Offset 3E - Minimum Grant (00h).................................... RO

Offset 3F - Maximum Latency (00h)................................ RO

IDE-Controller-Specific Configuration Registers

Offset 40 - Chip Enable (00h) .... RW

- **7-2 Reserved** .... always reads 0
- **1 Primary Channel**
  - 0 Disable .... default
  - 1 Enable
- **0 Secondary Channel**
  - 0 Disable .... default
  - 1 Enable

Offset 41 - IDE Configuration I (00h) .... RW

- **7 Primary IDE Read Prefetch Buffer**
  - 0 Disable .... default
  - 1 Enable
- **6 Primary IDE Post Write Buffer**
  - 0 Disable .... default
  - 1 Enable
- **5 Secondary IDE Read Prefetch Buffer**
  - 0 Disable .... default
  - 1 Enable
- **4 Secondary IDE Post Write Buffer**
  - 0 Disable .... default
  - 1 Enable
- **3-0 Reserved** .... always reads 0

Offset 42 - IDE Configuration II (00h) .... RW

- **7 PIO Operating Mode - Primary Channel**
  Selects the mode used in the primary channel for the I/O Base Address (not IRQ routing or sharing)
  - 0 Compatibility Mode (fixed addressing). default
  - 1 Native PCI Mode (flexible addressing)
- **6 PIO Operating Mode - Secondary Channel**
  Selects the mode used in the secondary channel for the I/O Base Address (not IRQ routing or sharing)
  - 0 Compatibility Mode (fixed addressing). default
  - 1 Native PCI Mode (flexible addressing)
- **5-0 Reserved** .... always reads 0

Offset 43 - FIFO Configuration (0Ah) .... RW

- **7-4 Reserved** .... always reads 0
- **3-2 Primary Channel FIFO Threshold**
  Determines the threshold required before the primary channel FIFO is flushed.
  - 00 FIFO flushed when 1/4 full
  - 01 FIFO flushed when 1/2 full
  - 10 FIFO flushed when 3/4 full .... **default**
  - 11 FIFO flushed when completely full (32 DWs)
- **1-0 Secondary Channel FIFO Threshold**
  Determines the threshold required before the secondary channel FIFO is flushed.
  - 00 FIFO flushed when 1/4 full
  - 01 FIFO flushed when 1/2 full
  - 10 FIFO flushed when 3/4 full .... **default**
  - 11 FIFO flushed when completely full (32 DWs)

Offset 44 - Miscellaneous Control 1 (08h) ....RW

7-5 Reserved .... always reads 0

4 PIO Read Pre-Fetch Byte Counter
Determines whether the amount of data prefetched under PIO read is limited.
- 0 Disable (no limit) .... default
- 1 Enable. The maximum number of bytes that can be prefetched is determined by Rx61-60[11:0] for the primary channel and Rx69-68[11:0] for the secondary channel.

3 Bus Master IDE Status Register Read Retry
Determines whether a read to the bus master IDE status register is retried when DMA operation is not complete.
- 0 Disable. Reads will return status even if DMA operation is not complete.
- 1 Enable. Reads of the status register are automatically retried while DMA operation is not complete. **..default**

2 Packet Command Prefetching
Determines whether prefetching is enabled for packet commands. Packet commands are commands for ATAPI, which is used for operating devices such as CD-ROM drives.
- 0 Disable .... default
- 1 Enable

1 Reserved .... always reads 0

0 UltraDMA Host Must Wait for First Transfer Before Termination
- 0 Enable. The UltraDMA host must wait until at least the first transfer is completed before it can terminate a transaction. .... default
- 1 Disable

Offset 45 - Miscellaneous Control 2 (20h)....................... RW

7 Reserved ....always reads 0

6 Interrupt Steering Swap
Controls whether primary and secondary channel interrupts are swapped.
- 0 Primary channel interrupt is steered to IRQ14, Secondary channel is steered to IRQ15 . default
- 1 Primary channel interrupt is steered to IRQ15, Secondary channel interrupt steered to IRQ14

5 Reserved .... always reads 1

4 Rx3C Write Protect
- 0 Disable (writes to Rx3C are allowed).... default
- 1 Enable (writes to Rx3C are ignored). Under Native Mode (Rx9[2]=1 or Rx9[0]=1) Rx3C should not be write protected as it is used to route IRQ lines.

3 "Memory-Read-Multiple" Command
- 0 Disable .... default
- 1 Enable

2 "Memory-Write-and-Invalidate" Command
- 0 Disable .... default
- 1 Enable

1-0 Reserved ....always reads 0

Offset 46 - Miscellaneous Control 3 (C0h)...................... RW

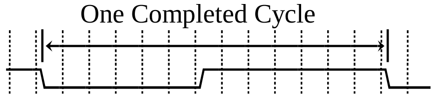
7 Primary Channel Read DMA FIFO Flush
- 0 Disable
- 1 Enable. The primary channel DMA FIFO is flushed when an interrupt request is generated **.. default**

6 Secondary Channel Read DMA FIFO Flush
- 0 Disable
- 1 Enable. The secondary channel DMA FIFO is flushed when an interrupt request is generated **.. default**

5-0 Reserved ....always reads 0

<u>Offset 4B-48 - Drive Timing Control (A8A8A8A8h)......RW</u>

The following fields define the Active Pulse Width and Recovery Time for the IDE DIOR# and DIOW# signals when accessing the data ports (1F0 and 170):



31-28 Primary Drive 0 Active Pulse Width...... def=1010b
27-24 Primary Drive 0 Recovery Time............ def=1000b
23-20 Primary Drive 1 Active Pulse Width...... def=1010b
19-16 Primary Drive 1 Recovery Time............ def=1000b
15-12 Secondary Drive 0 Active Pulse Width .. def=1010b
11-8 Secondary Drive 0 Recovery Time .... def=1000b
7-4 Secondary Drive 1 Active Pulse Width .. def=1010b
3-0 Secondary Drive 1 Recovery Time .... def=1000b

The actual value for each field is the encoded value in the field plus one and indicates the number of PCI clocks. For example, if the value in the field is 1010b (10 decimal), the active pulse width or recovery time is 11 PCI clocks.

<u>Offset 4C - Address Setup Time (FFh)............................RW</u>

The following fields define the Address Setup Time. The Address Setup Time is measured from the point when address signals are stable to the point when DIOR# and DIOW# are asserted. The IDE specification requires the setup time to not exceed 1T. However, the VT8233 provides flexibility for devices that may not be able to meet the 1T requirement.

7-6 Primary Drive 0 Address Setup Time
5-4 Primary Drive 1 Address Setup Time
3-2 Secondary Drive 0 Address Setup Time
1-0 Secondary Drive 1 Address Setup Time

For each field above:
00 1T
01 2T
10 3T
11 4T **...default**

<u>Offset 4E – Sec Non-1F0 Port Access Timing (B6h).......RW</u>

7-4 DIOR# / DIOW# Active Pulse Width.......def = 0Bh
3-0 DIOR# / DIOW# Recovery Time.............. def = 06h

<u>Offset 4F – Pri Non-1F0 Port Access Timing (B6h) ....RW</u>

7-4 DIOR# / DIOW# Active Pulse Width.......def = 0Bh
3-0 DIOR# / DIOW# Recovery Time.............. def = 06h

The above fields define the primary and secondary channel DIOR# and DIOW# active pulse widths and recovery times when accessing non-data ports. The times are defined in terms of PCI clocks and the actual value is equal to the value encoded in the field plus one.

<u>Offset 53-50 - UltraDMA Extended Timing Control..... RW</u>

31 Pri Drive 0 UltraDMA-Mode Enable Method
0 Enable by using "Set Feature" command .... def
1 Enable by setting bit-30 of this register
30 Pri Drive 0 UltraDMA-Mode Enable
0 Disable... default
1 Enable UltraDMA-Mode Operation
29 Pri Drive 0 Transfer Mode
0 DMA or PIO Mode .... default
1 UltraDMA Mode
28 Pri Drive 0 Cable Type Reporting
0 40-pin cable is being used...................... default
1 80-pin cable is being used
27-24 Pri Drive 0 Cycle Time (T = 7.5 ns for 133 MHz)

0000	2T	
0001	3T	
0010	4T	
0011	5T	
0100	6T	
0101	7T	
0110	8T	
0111	9T	.... default
1000	10T	
1001	11T	
1010	12T	
1011	13T	
1100	14T	
1101	15T	
1110	16T	
1111	17T	

23 Pri Drive 1 UltraDMA-Mode Enable Method
22 Pri Drive 1 UltraDMA-Mode Enable
21 Pri Drive 1 Transfer Mode
20 Pri Drive 1 Cable Type Reporting
0 40-pin cable is being used...................... default
1 80-pin cable is being used
19-16 Pri Drive 1 Cycle Time...................default = 0111b

15 Sec Drive 0 UltraDMA-Mode Enable Method
14 Sec Drive 0 UltraDMA-Mode Enable
13 Sec Drive 0 Transfer Mode
12 Sec Drive 0 Cable Type Reporting
0 40-pin cable is being used...................... default
1 80-pin cable is being used
11-8 Sec Drive 0 Cycle Time ....default = 0111b

7 Sec Drive 1 UltraDMA-Mode Enable Method
6 Sec Drive 1 UltraDMA-Mode Enable
5 Sec Drive 1 Transfer Mode
4 Sec Drive 1 Cable Type Reporting
0 40-pin cable is being used...................... default
1 80-pin cable is being used
3-0 Sec Drive 1 Cycle Time ....default = 0111b

Each byte defines UltraDMA operation for the indicated drive. The bit definitions are the same within each byte.

Offset 54 – UltraDMA FIFO Control (04h) ....RW

- **7 Reserved** .... always reads 0
- **6 Lower ISA Request Priority When Write Device Packet Command is Issued**
  The IDE secondary channel shares a bus internally with the ISA interface. When this bit is enabled, the IDE secondary channel is given higher priority over ISA, which results in better performance.
  - 0 Disable .... default
  - 1 Enable
- **5 Clear Native Mode Interrupt on Falling Edge of Gated Interrupt**
  - 0 Disable .... default
  - 1 Enable. The interrupt will be automatically cleared on the falling edge of the gated interrupt.
- **4 Improve PIO Prefetch and Post-Write Performance**
  - 0 Enable. PIO prefetch and post write performance is increased by being given higher throughput. .... default
  - 1 Disable
- **3 Memory Prefetch Size**
  This bit determines how many lines are prefetched from memory for IDE transactions.
  - 0 Prefetch 1 line .... default
  - 1 Prefetch 2 lines (16 DoubleWords). This setting improves ATA100 throughput.
- **2 Change Drive Clears All FIFO & Internal States**
  - 0 Disable
  - 1 Command switch from one drive to another drive in the same channel terminates all previous outstanding transactions involving the previous drive. **................................default**
- **1 Reserved** .... always reads 0
- **0 Complete DMA Cycle with Transfer Size Less Than FIFO Size**
  - 0 Enable. DMA transfer size is less than the FIFO size .... default
  - 1 Disable

Offset 55 – IDE Clock Gating (00h) .... RW

- **7-2 Reserved** ....always reads 0
- **1 Dynamic 100 / 133 MHz Clock Gating**
  - 0 Enable .... default
  - 1 Disable
- **0 Dynamic 66 MHz Clock Gating**
  - 0 Enable .... default
  - 1 Disable

Offset 61-60 - Primary Sector Size (0200h) .... RW

- **15-12 Reserved** ....always reads 0
- **11-0 Number of Bytes Per Sector** ...def=200h (512 bytes)
  This field determines the maximum number of bytes that can be prefetched when Rx44[4] = 1.

Offset 69-68 - Secondary Sector Size (0200h)................. RW

- **15-12 Reserved** ....always reads 0
- **11-0 Number of Bytes Per Sector** ...def=200h (512 bytes)
  This field determines the maximum number of bytes that can be prefetched when Rx44[4] = 1.

Offset 70 – Primary IDE Status .... RO

- **7 Interrupt Status.. RO**
  - 1 Primary channel interrupt request pending
- **6 Prefetch Buffer Status .... RO**
  - 1 PIO Prefetch transaction in progress
- **5 Post Write Buffer Status.................................... RO**
  - 1 PIO Post Write transaction in progress
- **4 DMA Read Prefetch Status .... RO**
  - 1 DMA Read Prefetch transaction in progress
- **3 DMA Write Pipeline Status................................ RO**
  - 1 DMA Write transaction in progress
- **2 S/G Operation Complete .... RO**
  - 1 Scatter / Gather operation complete
- **1 FIFO Empty Status... RO**
  - 1 Primary Channel FIFO empty
- **0 Response to External DMA Request .... RO**
  - 1 External pri channel DMA request pending

Offset 71 – Primary Interrupt Control (01h)..................RW

- **7-1 Reserved** .... always reads 0
- **0 Interrupt Gating**
  - 0 Disable
  - 1 Enable (IRQ output gated until FIFO empty) **..default**

Offset 78 – Secondary IDE Status.................................... RO

- **7 Interrupt Status.. RO**
  - 1 Secondary channel interrupt request pending
- **6 Prefetch Buffer Status .... RO**
  - 1 PIO Prefetch transaction in progress
- **5 Post Write Buffer Status.................................... RO**
  - 1 PIO Post Write transaction in progress
- **4 DMA Read Prefetch Status .... RO**
  - 1 DMA Read Prefetch transaction in progress
- **3 DMA Write Pipeline Status................................ RO**
  - 1 DMA Write transaction in progress
- **2 S/G Operation Complete .... RO**
  - 1 Scatter / Gather operation complete
- **1 FIFO Empty Status... RO**
  - 1 Secondary Channel FIFO empty
- **0 Response to External DMA Request .... RO**
  - 1 External sec channel DMA request pending

Offset 79 - Secondary Interrupt Control (01h)...............RW

- **7-1 Reserved** .... always reads 0
- **0 Interrupt Gating**
  - 0 Disable
  - 1 Enable (IRQ output gated until FIFO empty) **..default**

Offset 83-80 – Primary S/G Descriptor Address .... RO

Offset 8B-88 – Secondary S/G Descriptor Address .... RO

These registers are used for debugging purposes only.

IDE Power Management Registers

Offset C3-C0 – Power Management Capabilities .... RO

- **31-0 PCI PM Block 1** .... always reads 0002 0001h
  This field reports support details for Power Management Capabilities according to the PCI Power Management specification.

Offset C7-C4 – Power State .... RO

- **31-2 Reserved** .... always reads 0
- **1-0 Power State**
  - 00 D0 .... default
  - 01 -reserved-
  - 10 -reserved-
  - 11 D3 Hot

IDE Back Door Registers

Offset D0 – Back Door – Revision ID (06h).................... RW

Offset D3-D2 – Back Door – Device ID (0571h) .... RW

Offset D5-D4 – Back Door – Sub-Vendor ID (0000h).... RW

Offset D7-D6 – Back Door – Sub-Device ID (0000h) ..... RW

IDE Revision ID

Offset F6 – IDE New Revision ID (07h) .... RO

IDE I/O Registers

These registers are compliant with the SFF 8038I v1.0 standard. Refer to the SFF 8038I v1.0 specification for further details.

I/O Offset 0 - Primary Channel Command

I/O Offset 2 - Primary Channel Status

I/O Offset 4-7 - Primary Channel PRD Table Address

I/O Offset 8 - Secondary Channel Command

I/O Offset A - Secondary Channel Status

I/O Offset C-F - Secondary Channel PRD Table Address

Device 17 Function 5 Registers - AC97 Audio Controller

The audio controller interface is hardware compatible with AC97. The PCI configuration registers for the audio controller are located in the function 5 PCI configuration space. The I/O registers are located in the system I/O space.

PCI Configuration Space Header

Offset 1-0 - Vendor ID .... RO

7-0	**Vendor ID**	.... (1106h = VIA Technologies)

Offset 3-2 - Device ID .... RO

7-0	**Device ID**	(3059h = VT8235 Audio Controller)

Offset 5-4 - Command .... RW

15-10	**Reserved**	.... always reads 0
9	**Reserved** (fast back-to-back)	.... fixed at 0
8	**SERR# Enable**	.... fixed at 0
7	**Reserved** (address stepping)	.... fixed at 0
6	**Reserved** (parity error response)	.... fixed at 0
5	**Reserved** (VGA palette snoop)	.... fixed at 0
4	**Reserved** (memory write and invalidate)	.... fixed at 0
3	**Reserved** (special cycle monitoring)	.... fixed at 0
2	**Bus Master**	.... fixed at 0
1	**Memory Space**	.... fixed at 0
0	**I/O Space**	.... default=0 (disabled)

Offset 7-6 - Status .... RO

15	**Detected Parity Error**	.... fixed at 0
14	**Signalled System Error**	.... fixed at 0
13	**Received Master Abort**	.... fixed at 0
12	**Received Target Abort**	.... fixed at 0
11	**Signalled Target Abort**	.... fixed at 0
10-9	**DEVSEL# Timing**	
	00 Fast	
	01 Medium	.... fixed
	10 Slow	
	11 Reserved	
8	**Data Parity Error**	.... fixed at 0
7	**Fast Back-to-Back Capable**	.... fixed at 0
6-5	**Reserved**	.... always reads 0
4	**PM 1.1**	.... fixed at 1
3-0	**Reserved**	.... always reads 0

Offset 8 - Revision ID (nnh) .... RO

7-0	**Silicon Revision Code**	.... default = nnh

Offset 9 - Programming Interface (00h) .... **RO**

Offset A - Sub Class Code (01h=Audio Device)............... **RO**

Offset B - Base Class Code (04h=Multimedia Device)..... **RO**

Offset 13-10 - Base Address 0 – SGD Control / Status .. RW

31-16	**Reserved**	....always reads 0
15-8	**Base Address**	....default = 00h
7-0	**00000001b (256 bytes)**	

Device 0 Offset 2D-2C – Subsystem Vendor ID (0000h)*RO

15-0	**Subsystem Vendor ID**	.............................default = 0

*This register is RW if function 5-6 Rx44[4] = 1

Device 0 Offset 2F-2E – Subsystem ID (0000h)............. *RO

15-0	**Subsystem ID**	....default = 0

*This register is RW if function 5-6 Rx44[4] = 1

Offset 34 – Capture Pointer (C0h) .... RO

Offset 3C - Interrupt Line.. RW

7-4	**Reserved**	....always reads 0
3-0	**Audio Interrupt Routing**	
	0000 Disabled	.... default
	0001 IRQ1	
	0010 Reserved	
	0011 IRQ3	
	0100 IRQ4	
	0101 IRQ5	
	0110 IRQ6	
	0111 IRQ7	
	1000 IRQ8	
	1001 IRQ9	
	1010 IRQ10	
	1011 IRQ11	
	1100 IRQ12	
	1101 IRQ13	
	1110 IRQ14	
	1111 Disabled	
	APIC (See Device 17 Function 0 Rx4D[7])	
	x000 IRQ16	
	x001 IRQ17	
	x010 IRQ18	
	… …	
	x111 IRQ23	

Offset 3D - Interrupt Pin (03h) .... **RO**

Offset 3E - Minimum Grant (00h)................................... **RO**

Offset 3F - Maximum Latency (00h) .... **RO**

Audio-Specific PCI Configuration Registers

Offset 40 – AC Link Interface Status .... RO

7-6 Reserved .... always reads 0

5 Codec CID=11b Ready Status........................... RO
- 0 Codec Not Ready
- 1 Codec Ready (audio ctrlr can access codec)

4 Codec CID=10b Ready Status........................... RO
- 0 Codec Not Ready
- 1 Codec Ready (audio ctrlr can access codec)

3 Reserved .... always reads 0

2 Codec CID=01b Ready Status........................... RO
- 0 Codec Not Ready
- 1 Codec Ready (audio ctrlr can access codec)

1 AC97 Low-Power Status .... RO
- 0 AC97 Codecs not in low-power mode
- 1 AC97 Codecs in low-power mode

This bit reports 1 when Rx26[4] of the codecs is 1. It is used to determine whether the bit-clock should be gated.

0 Codec CID=00b Ready Status........................... RO
- 0 Codec Not Ready
- 1 Codec Ready (audio ctrlr can access codec)

Offset 41 – AC Link Interface Control .... RW

7 AC-Link Interface
- 0 Disable .... default
- 1 Enable

6 AC-Link Reset

0Assert AC-Link Reset (used for cold reset).......... def

1De-assert AC-Link Reset

5 AC-Link Sync
- 0 Release SYNC .... default
- 1 Force SYNC High (used for warm reset)

4 AC-Link Serial Data Out
- 0 Release SDO... default
- 1 Force SDO High

3 Variable-Sample-Rate On-Demand Mode
- 0 Disable (AC Link sends data every frame).. def
- 1 Enable (AC Link sends data only when there is a request from the codec)

2 3D Audio Channel Slots 3/4
- 0 Disable .... default
- 1 Enable

Note that slots 7/8 and 6/9 do not have to be selected as they are not muxed with DXS as are slots 3/4)

1-0 Reserved .... always reads 0

Offset 42 – Function Enable ....RW

- **7-6 Reserved** .... always reads 0
- **5 Function 5 Config Reg Rx2C Writable ....RW**
  - 0 Device 17 Function 5 Rx2C-2F RO ...... default
  - 1 Device 17 Function 5 Rx2C-2F RW
- **4-0 Reserved** .... always reads 0

Offset 44 – MC97 Interface Control .... RO

Mapped RO to function 5 (RW in func 6) for status reporting.

- **7 AC-Link Interface for Slot-5 (Modem) .... RO**
  - 0 Disable .... default
  - 1 Enable
- **6 Secondary Codec Support .... RO**
  - 0 Disable .... default
  - 1 Enable
- **5 Function 6 Config Reg Rx9-B Writable .... RO**
  - 0 Device 17 Function 6 Rx9-B RO .... default
  - 1 Device 17 Function 6 Rx9-B RW
- **4 Function 6 Config Reg 2Ch Writable .... RO**
  - 0 Device 17 Function 6 Rx2C-2F RO ...... default
  - 1 Device 17 Function 6 Rx2C-2F RW
- **3 Sync .... RO**
  This bit reports whether there is activity in function 6 (modem). When function 5 (audio) enters low-power state and wants to gate bit-clock, software needs to check this bit to see whether bit-clock can actually be gated, as function 6 shares the same bit-clock.
  - 0 Function 6 activity in progress that requires bit-clock
  - 1 Function 6 does not need bit-clock so bit-clock can be gated
- **2-0 Reserved** .... always reads 0

Offset 48 – Volume Change Rate Control .... RW

- **7-4 Volume Change Rate**
  This field controls the volume change rate in the sample rate converter
  - 0000 Volume Adjust Every Frame (sync cycle)...def
  - …
  - 1111 Volume Adjust Every 16 Frames (sync cycles)
- **3 Sync**
  This bit reports whether there is activity in function 5 (audio). When function 6 (modem) enters low-power state and wants to gate bit-clock, software needs to check this bit to see whether bit-clock can actually be gated, as function 5 shares the same bit-clock.
  - 0 Function 5 activity in progress that requires bit-clock
  - 1 Function 5 does not need bit-clock so bit-clock can be gated
- **2-0 Reserved** .... **RW**

Offset 49 – S/PDIF Control .... RW

- **7-4 Reserved** ....always reads 0
- **3 DX3 (DirectSound) Channel S/PDIF Support**
  This bit controls whether DirectSound Channel 3 is used as S/PDIF support
  - 0 Disable .... default
  - 1 Enable
- **2 Reserved** ....always reads 0
- **1-0 S/PDIF Data Slot Select**
  - 00 Slot 10/11... default
  - 01 Slot 3/4
  - 10 Slot 7/8
  - 11 Slot 6/9

Offset C3-C0 – Power Mgmt Capability......................... RO

- **31-0 Power Mgmt Capability**.... always reads 0002 0001h

Offset C7-C4 – Power State .... RW

- **31-2 Reserved** ....always reads 0
- **1-0 Power State (D3 / D0 Only)**

I/O Base 0 Regs – Audio Scatter / Gather DMA

DXS Channel 0-3 SGD Registers (x = 0-3)

I/O Offset x0 – DXS Channel x SGD Status.................RWC

7 SGD Active .... RO
- 0 SGD has completed or been terminated default
- 1 SGD Active

6-5 Reserved .... always reads 0

4 Current SGD Index Equals Stop Index .... RO
- 0 SGD index not equal to stop index........ default
- 1 SGD index being processed equals the stop index. This bit differs from bit-2 of this register in that this bit becomes 1 as soon as the SGD *reaches* the index equal to the stop index. Bit-2 becomes 1 after the SGD *finishes processing* the index equal to the stop index. So this bit will always turn on before bit-2.

3 SGD Trigger Queued.. RO
This bit reports whether the trigger used to restart the SGD operation is queued (I/O Offset x1[1] = 1 while the SGD engine is running).
- 0 SGD trigger not queued......................... default
- 1 SGD trigger queued (when SGD reaches EOL, it will restart).

2 SGD Stop Interrupt Status..............................RWC
- 1 SGD finished the index equal to the stop index set in xB-x8[31-24].

1 SGD EOL (End Of Link)................................RWC
- 1 Block is the last of the link. May be used by software as a signal to generate an interrupt request if I/O Offset x1[1] = 1.

0 SGD Flag ....RWC
- 1 Block complete. May be used by software as a signal to generate an interrupt request if I/O Offset x1[0] = 1.

I/O Offset x1 – DXS Channel x SGD Control .... RW

7 SGD Start ....WO (always reads 0)
- 0 No effect
- 1 Start SGD operation

6 SGD Terminate.......................WO (always reads 0)
- 0 No effect
- 1 Terminate SGD operation

5 SGD Auto-Start
- 0 Stop at EOL .... default
- 1 Auto Restart at EOL

4 Reserved ....always reads 0

3 SGD Pause
- 0 Release pause and resume the transfer
- 1 Pause SGD read operation (SGD pointer stays at the current address). SGD will finish transferring the current block before pausing.

2 Interrupt on Stop Index = Current Index and End of Block
Controls whether an interrupt is generated when the current index equals the stop index (x0[2] = 1).
- 0 Disable .... default
- 1 Enable

1 Interrupt on EOL @ End of Block
Controls whether an interrupt is generated on EOL (x0[1] = 1).
- 0 Disable .... default
- 1 Enable

0 Interrupt on FLAG @ End-of-Block
Controls whether an interrupt is generated on FLAG (x0[0] = 1).
- 0 Disable .... default
- 1 Enable

I/O Offset x2 – DXS Left Channel x Volume (3Fh)........RW

I/O Offset x3 – DXS Right Channel x Volume (3Fh) .....RW

7-6 Reserved (Do Not Program)............always write 0's

5-0 Volume Control

000000	0 db
…	…
000111	-10.5 db
…	…
011111	-46.5 db
…	…
111111	Muted (instead of -94.5 db) .... default

I/O Offset x7-x4 – DXS Chan x SGD Table Ptr Base.....RW

31-0 SGD Table Pointer Base Address (even addr).... W
Current Pointer Address ....R

I/O Offset xB-x8 – StopIndex / DataType / SampleRate RW

31-24 SGD Stop Index Setting.......................default = FFh

23-22 Reserved .... always reads 0

21-20 PCM Format

Selects the format used by the controller to process the incoming sample.

- 00 8-bit Mono... default
- 01 8-bit Stereo
- 10 16-bit Mono
- 11 16-bit Stereo

19-0 Sample Rate.........................default = FFFFFh (48K)

This field allows the sample rate converter to know the sample rate of an incoming sample so the converter can properly convert the sample into the required 48 KHz sample output. Program as (2^{20} / 48.000) * Sample Rate

I/O Offset xF-xC – DXS Chan x SGD Current Count.... RO

31-24 Current SGD Index

This field reports the index the SGD engine is currently processing.

23-0 Current SGD Count

This field reports the count remaining in the current entry being processed. For example, if 10 bytes of a 30-byte count have been transferred, this field would read 20 to indicate 20 bytes remaining.

Audio SGD Table Format

63	62	61-56	55-32	31-0
EOL	FLAG	-reserved-	Base Count [23:0]	Base Address [31:0]

EOL End Of Link. 1 indicates this block is the last of the link. If the channel "Interrupt on EOL" bit is set, then an interrupt is generated at the end of the transfer.

FLAG Block Flag. If set, transfer pauses at the end of this block. If the channel "Interrupt on FLAG" bit is set, then an interrupt is generated at the end of this block.

Multichannel SGD Registers

I/O Offset 40 – Multichannel SGD Status ....RWC

- **7 SGD Active .... RO**
  - 0 SGD has completed or been terminated default
  - 1 SGD Active
- **6-5 Reserved** .... always reads 0
- **4 Current SGD Index Equals Stop Index .... RO**
  - 0 SGD index not equal to stop index........ default
  - 1 SGD index being processed equals the stop index. This bit differs from bit-2 of this register in that this bit becomes 1 as soon as the SGD *reaches* the index equal to the stop index. Bit-2 becomes 1 after the SGD *finishes processing* the index equal to the stop index. So this bit will always turn on before bit-2.
- **3 SGD Trigger Queued .... RO**
  This bit reports whether the trigger used to restart the SGD operation is queued (I/O Offset 41[1] = 1 while the SGD engine is running).
  - 0 SGD trigger not queued......................... default
  - 1 SGD trigger queued (when SGD reaches EOL, it will restart).
- **2 SGD Stop Interrupt Status..............................RWC**
  - 1 SGD finished the index equal to the stop index set in 4B-48[31-24].
- **1 SGD EOL (End Of Link).................................RWC**
  - 1 Block is the last of the link. May be used by software as a signal to generate an interrupt request if I/O Offset 41[1] = 1.
- **0 SGD Flag ....RWC**
  - 1 Block complete. May be used by software as a signal to generate an interrupt request if I/O Offset 41[0] = 1.

I/O Offset 41 – Multichannel SGD Control.................... RW

- **7 SGD Start ....WO (always reads 0)**
  - 0 No effect
  - 1 Start SGD operation
- **6 SGD Terminate.......................WO (always reads 0)**
  - 0 No effect
  - 1 Terminate SGD operation
- **5 SGD Auto-Start**
  - 0 Stop at EOL .... default
  - 1 Auto Restart at EOL
- **4 Reserved** .... always reads 0
- **3 SGD Pause**
  - 0 Release pause and resume the transfer
  - 1 Pause SGD read operation (SGD pointer stays at the current address). SGD will finish transferring the current block before pausing.
- **2 Interrupt on Stop Index = Current Index and End of Block**
  Controls whether an interrupt is generated when the current index equals the stop index (40[2] = 1).
  - 0 Disable .... default
  - 1 Enable
- **1 Interrupt on EOL @ End of Block**
  Controls whether an interrupt is generated on EOL (40[1] = 1).
  - 0 Disable .... default
  - 1 Enable
- **0 Interrupt on FLAG @ End-of-Block**
  Controls whether an interrupt is generated on FLAG (40[0] = 1).
  - 0 Disable .... default
  - 1 Enable

I/O Offset 42 – Multichannel SGD Format.....................RW

7 PCM Format
Selects the PCM format used by the controller to process the incoming sample.
0 8-bit .... default
1 16-bit

6-4 Number of Channels Supported
000 -reserved-.. default
001 One Channel
010 Two Channels
011 Three Channels
100 Four Channels
101 Five Channels
110 Six Channels
111 -reserved-

3-0 Reserved .... always reads 0

I/O Offset 43 – Multichannel Scratch Register...............RW

7-0 No Hardware Function........................ default = 00h

I/O Offset 47-44 – Multichannel SGD Table Ptr Base ...RW

31-0 SGD Table Pointer Base Address (even addr).... W
Current Pointer Address ....R

I/O Offset 4B-48 – Multichannel SGD Slot Select.......... RW

31-24 SGD Stop Index Setting .... default = FFh

23-20 Data Select of Slot 9
0 No data assigned to slot 9 .... default
1 1st data in sample assigned to slot 9
2 2nd data in sample assigned to slot 9
3 3rd data in sample assigned to slot 9
4 4th data in sample assigned to slot 9
5 5th data in sample assigned to slot 9
6 6th data in sample assigned to slot 9
7-F -reserved

19-16 Data Select of Slot 6

15-12 Data Select of Slot 8

11-8 Data Select of Slot 7

7-4 Data Select of Slot 4

3-0 Data Select of Slot 3

I/O Offset 4F-4C – Multichannel SGD Current Count .. RO

31-24 Current SGD Index
This field reports the index the SGD engine is currently processing.

23-0 Current SGD Count
This field reports the count remaining in the current entry being processed. For example, if 10 bytes of a 30-byte count have been transferred, this field would read 20 to indicate 20 bytes remaining.

Write Channel 0 SGD Registers

I/O Offset 60 – Write Channel 0 SGD Status..............RWC

- **7 SGD Active .... RO**
  - 0 SGD has completed or been terminated default
  - 1 SGD Active
- **6 SGD Paused .... RO**
  - 0 SGD not paused.................................... default
  - 1 SGD Paused
- **5 Reserved** .... always reads 0
- **4 Current SGD Index Equals Stop Index .... RO**
  - 0 SGD index not equal to stop index........ default
  - 1 SGD index being processed equals the stop index. This bit differs from bit-2 of this register in that this bit becomes 1 as soon as the SGD *reaches* the index equal to the stop index. Bit-2 becomes 1 after the SGD *finishes processing* the index equal to the stop index. So this bit will always turn on before bit-2.
- **3 SGD Trigger Queued .... RO**

  This bit reports whether the trigger used to restart the SGD operation is queued (I/O Offset 61[1] = 1 while the SGD engine is running).
  - 0 SGD trigger not queued......................... default
  - 1 SGD trigger queued (when SGD reaches EOL, it will restart).
- **2 SGD Stop Interrupt Status.............................RWC**
  - 1 SGD finished the index equal to the stop index set in 6B-68[31-24].
- **1 SGD EOL (End Of Link)................................RWC**
  - 1 Block is the last of the link. May be used by software as a signal to generate an interrupt request if I/O Offset 61[1] = 1.
- **0 SGD Flag ....RWC**
  - 1 Block complete. May be used by software as a signal to generate an interrupt request if I/O Offset 61[0] = 1.

I/O Offset 61 – Write Channel 0 SGD Control .... RW

- **7 SGD Start ....WO (always reads 0)**
  - 0 No effect
  - 1 Start SGD operation
- **6 SGD Terminate.......................WO (always reads 0)**
  - 0 No effect
  - 1 Terminate SGD operation
- **5 SGD Auto-Start**
  - 0 Stop at EOL .... default
  - 1 Auto Restart at EOL
- **4 Reserved** .... always reads 0
- **3 SGD Pause**
  - 0 Release pause and resume the transfer
  - 1 Pause SGD read operation (SGD pointer stays at the current address). SGD will finish transferring the current block before pausing.
- **2 Interrupt on Stop Index = Current Index and End of Block**

  Controls whether an interrupt is generated when the current index equals the stop index (60[2] = 1).
  - 0 Disable .... default
  - 1 Enable
- **1 Interrupt on EOL @ End of Block**

  Controls whether an interrupt is generated on EOL (60[1] = 1).
  - 0 Disable .... default
  - 1 Enable
- **0 Interrupt on FLAG @ End-of-Block**

  Controls whether an interrupt is generated on FLAG (60[0] = 1).
  - 0 Disable .... default
  - 1 Enable

I/O Offset 62 – Write Channel 0 SGD Format ....RW

- **7** **Reserved (Do Not Program)** ....always write 0
- **6** **Recording FIFO**
  - 0 Disable .... default
  - 1 Enable
- **5-0** **Reserved** .... always reads 0

I/O Offset 63 – Write Channel 0 Input Select ....RW

- **7-3** **Reserved** .... always reads 0
- **2** **Input Source Select**
  - 0 Line In (Slot 3, 4) .... default
  - 1 Mic In (Slot 6)
- **1-0** **Recording Source Select**
  - 00 Primary Codex .... default
  - 01 Secondary Codec 01
  - 10 Secondary Codec 10
  - 11 Secondary Codec 11

I/O Offset 67-64 – Wr Channel 0 SGD Table Ptr Base ..RW

- **31-0** **SGD Table Pointer Base Address (even addr).... W**
  Current Pointer Address ....R

I/O Offset 6B-68 – Write Channel 0 SGD Stop Index ... RW

- **31-24** **SGD Stop Index Setting** .... default = FFh
- **23-22** **Reserved** ....always reads 0
- **21-20** **PCM Format**
  Selects the PCM format used by the controller to process the incoming sample.
  - 00 8-bit Mono ....default
  - 01 8-bit Stereo
  - 10 16-bit Mono
  - 11 16-bit Stereo
- **19-16** **Reserved** **... RW**
- **15-0** **Reserved** ....always reads 0

I/O Offset 6F-6C – Wr Channel 0 SGD Current Count . RO

- **31-24** **Current SGD Index**
  This field reports the index the SGD engine is currently processing.
- **23-0** **Current SGD Count**
  This field reports the count remaining in the current entry being processed. For example, if 10 bytes of a 30-byte count have been transferred, this field would read 20 to indicate 20 bytes remaining.

Write Channel 1 SGD Registers

I/O Offset 70 – Write Channel 1 SGD Status ....RWC

- **7 SGD Active .... RO**
  - 0 SGD has completed or been terminated default
  - 1 SGD Active
- **6 SGD Paused .... RO**
  - 0 SGD not paused.................................... default
  - 1 SGD Paused
- **5 Reserved** .... always reads 0
- **4 Current SGD Index Equals Stop Index .... RO**
  - 0 SGD index not equal to stop index........ default
  - 1 SGD index being processed equals the stop index. This bit differs from bit-2 of this register in that this bit becomes 1 as soon as the SGD *reaches* the index equal to the stop index. Bit-2 becomes 1 after the SGD *finishes processing* the index equal to the stop index. So this bit will always turn on before bit-2.
- **3 SGD Trigger Queued .... RO**
  This bit reports whether the trigger used to restart the SGD operation is queued (I/O Offset 71[1] = 1 while the SGD engine is running).
  - 0 SGD trigger not queued......................... default
  - 1 SGD trigger queued (when SGD reaches EOL, it will restart).
- **2 SGD Stop Interrupt Status.............................RWC**
  - 1 SGD finished the index equal to the stop index set in 7B-78[31-24].
- **1 SGD EOL (End Of Link)................................RWC**
  - 1 Block is the last of the link. May be used by software as a signal to generate an interrupt request if I/O Offset 71[1] = 1.
- **0 SGD Flag ....RWC**
  - 1 Block complete. May be used by software as a signal to generate an interrupt request if I/O Offset 71[0] = 1.

I/O Offset 71 – Write Channel 1 SGD Control .... RW

- **7 SGD Start ....WO (always reads 0)**
  - 0 No effect
  - 1 Start SGD operation
- **6 SGD Terminate.......................WO (always reads 0)**
  - 0 No effect
  - 1 Terminate SGD operation
- **5 SGD Auto-Start**
  - 0 Stop at EOL .... default
  - 1 Auto Restart at EOL
- **4 Reserved** ....always reads 0
- **3 SGD Pause**
  - 0 Release pause and resume the transfer
  - 1 Pause SGD read operation (SGD pointer stays at the current address). SGD will finish transferring the current block before pausing.
- **2 Interrupt on Stop Index = Current Index and End of Block**
  Controls whether an interrupt is generated when the current index equals the stop index (70[2] = 1).
  - 0 Disable .... default
  - 1 Enable
- **1 Interrupt on EOL @ End of Block**
  Controls whether an interrupt is generated on EOL (70[1] = 1).
  - 0 Disable .... default
  - 1 Enable
- **0 Interrupt on FLAG @ End-of-Block**
  Controls whether an interrupt is generated on FLAG (70[0] = 1).
  - 0 Disable .... default
  - 1 Enable

I/O Offset 72 – Write Channel 1 SGD Format ....RW

- **7 Reserved (Do Not Program)** ....always write 0
- **6 Recording FIFO**
  - 0 Disable .... default
  - 1 Enable
- **5-0 Reserved** .... always reads 0

I/O Offset 73 – Write Channel 1 Input Select ....RW

- **7-3 Reserved** .... always reads 0
- **2 Input Source Select**
  - 0 Line In (Slot 3, 4) .... default
  - 1 Mic In (Slot 6)
- **1-0 Recording Source Select**
  - 00 Primary Codex .... default
  - 01 Secondary Codec 01
  - 10 Secondary Codec 10
  - 11 Secondary Codec 11

I/O Offset 77-74 – Wr Channel 1 SGD Table Ptr Base ..RW

- **31-0 SGD Table Pointer Base Address (even addr).... W**
  Current Pointer Address ....R

I/O Offset 7B-78 – Write Channel 1 SGD Stop Index ... RW

- **31-24 SGD Stop Index Setting** .... default = FFh
- **23-22 Reserved** ....always reads 0
- **21-20 PCM Format**
  Selects the PCM format used by the controller to process the incoming sample.
  - 00 8-bit Mono ....default
  - 01 8-bit Stereo
  - 10 16-bit Mono
  - 11 16-bit Stereo
- **19-16 Reserved .... RW**
- **15-0 Reserved** ....always reads 0

I/O Offset 7F-7C – Wr Channel 1 SGD Current Count. RO

- **31-24 Current SGD Index**
  This field reports the index the SGD engine is currently processing.
- **23-0 Current SGD Count**
  This field reports the count remaining in the current entry being processed. For example, if 10 bytes of a 30-byte count have been transferred, this field would read 20 to indicate 20 bytes remaining.

Codec Command / Status SGD Registers

These registers are used to send commands to the codecs

I/O Offset 83-80 – AC97 Controller Cmd (W) / Status (R)

This register may be accessed from either function 5 or 6

31-30 Codec ID ....**RW**
- 00 Select Codec CID = 00
- 01 Select Codec CID = 01
- 10 Select Codec CID = 10
- 11 Select Codec CID = 11

29 Codec 11 Data / Status / Index Valid .... RO
- 0 Not Valid
- 1 Valid (OK to Read bits 0-23)

28 Codec 10 Data / Status / Index Valid .... RO
- 0 Not Valid
- 1 Valid (OK to Read bits 0-23)

27 Codec 01 Data / Status / Index Valid .... RO
- 0 Not Valid
- 1 Valid (OK to Read bits 0-23)

26 Reserved .... always reads 0

25 Codec 00 Data / Status / Index Valid .... RO
- 0 Not Valid
- 1 Valid (OK to Read bits 0-23)

24 AC97 Controller Busy .... RO
- 0 Codec is ready for a register access command
- 1 AC97 Controller is sending a command to the codec (commands are not accepted)

23 Codec Register Read / Write Mode ....**RW**
- 0 Select Codec register write mode
- 1 Select Codec register read mode

22-16 Codec Register Index [7:1] ....**RW**
Index of the AC97 codec register to access (in the attached codec). Data must be written before or at the same time as Index because writing to the index triggers the AC97 controller to access the addressed codec register over the AC-link interface.

15-0 Codec Register Data..**RW**

I/O Offset 87-84 – Audio SGD Status Shadow .... RO

31	**Audio Record 1 SGD Active Shadow**	**(Rx70[7])**
30	**Audio Record 1 SGD Stop Shadow**	**(Rx70[2])**
29	**Audio Record 1 SGD EOL Shadow**	**(Rx70[1])**
28	**Audio Record 1 SGD Flag Shadow**	**(Rx70[0])**
27	**Audio Record 0 SGD Active Shadow**	**(Rx60[7])**
26	**Audio Record 0 SGD Stop Shadow**	**(Rx60[2])**
25	**Audio Record 0 SGD EOL Shadow**	**(Rx60[1])**
24	**Audio Record 0 SGD Flag Shadow**	**(Rx60[0])**
23-20	**Reserved**	always reads 0
19	**MultiChannel SGD Active Shadow**	**(Rx40[7])**
18	**MultiChannel SGD Stop Shadow**	**(Rx40[2])**
17	**MultiChannel SGD EOL Shadow**	**(Rx40[1])**
16	**MultiChannel SGD Flag Shadow**	**(Rx40[0])**
15	**DX Channel 3 SGD Active Shadow**	**(Rx30[7])**
14	**DX Channel 3 SGD Stop Shadow**	**(Rx30[2])**
13	**DX Channel 3 SGD EOL Shadow**	**(Rx30[1])**
12	**DX Channel 3 SGD Flag Shadow**	**(Rx30[0])**
11	**DX Channel 2 SGD Active Shadow**	**(Rx20[7])**
10	**DX Channel 2 SGD Stop Shadow**	**(Rx20[2])**
9	**DX Channel 2 SGD EOL Shadow**	**(Rx20[1])**
8	**DX Channel 2 SGD Flag Shadow**	**(Rx20[0])**
7	**DX Channel 1 SGD Active Shadow**	**(Rx10[7])**
6	**DX Channel 1 SGD Stop Shadow**	**(Rx10[2])**
5	**DX Channel 1 SGD EOL Shadow**	**(Rx10[1])**
4	**DX Channel 1 SGD Flag Shadow**	**(Rx10[0])**
3	**DX Channel 0 SGD Active Shadow**	**(Rx00[7])**
2	**DX Channel 0 SGD Stop Shadow**	**(Rx00[2])**
1	**DX Channel 0 SGD EOL Shadow**	**(Rx00[1])**
0	**DX Channel 0 SGD Flag Shadow**	**(Rx00[0])**

I/O Offset 8B-88 – Codec GPI Interrupt Status / GPIO. RO

This register may be accessed from either function 5 or 6

31-16 GPI Interrupt Status .... **RO**
- R GPI[15-0] Interrupt Status
- W 1 to clear

15-0 Codec GPIO .... **RO**
- R Reflect status of Codec GPI[15-0]
- W Triggers AC-Link slot-12 output to codec

I/O Offset 8F-8C – Codec GPI Interrupt Enable .... RO

This register may be accessed from either function 5 or 6

31-16 Interrupt on GPI[15-0] Change of Status.......... **RO**
- 0 Disable
- 1 Enable

15-0 Reserved .... always reads 0

Offset 90-9F – Mapped from Function 5/6 Rx40-4F....... RO

Device 17 Function 6 Registers - AC97 Modem Controller

The modem controller interface is hardware compatible with AC97. The PCI configuration registers for the modem controller are located in the function 6 PCI configuration space. The I/O registers are located in the system I/O space.

PCI Configuration Space Header

Offset 1-0 - Vendor ID (1106h).. RO

7-0	**Vendor ID**	.... (1106h = VIA Technologies)

Offset 3-2 - Device ID (3068h) .... RO

7-0	**Device ID**	(3068h = VT8235 Modem Controller)

Offset 5-4 – Command (0000h) ....RW

15-10	**Reserved**	.... always reads 0
9	**Reserved** (fast back-to-back)	fixed at 0
8	**SERR# Enable**	fixed at 0
7	**Reserved** (address stepping)	fixed at 0
6	**Reserved** (parity error response)	fixed at 0
5	**Reserved** (VGA palette snoop)	fixed at 0
4	**Reserved** (memory write and invalidate)	fixed at 0
3	**Reserved** (special cycle monitoring)	fixed at 0
2	**Bus Master**	fixed at 0
1	**Memory Space**	fixed at 0
0	**I/O Space**	default=0 (disabled)

Offset 7-6 - Status (0200h) .... RO

15	**Detected Parity Error**	always reads 0
14	**Signalled System Error**	fixed at 0
13	**Received Master Abort**	fixed at 0
12	**Received Target Abort**	fixed at 0
11	**Signalled Target Abort**	fixed at 0
10-9	**DEVSEL# Timing**	
	00 Fast	
	01 Medium	fixed
	10 Slow	
	11 Reserved	
8	**Data Parity Error**	fixed at 0
7	**Fast Back-to-Back Capable**	fixed at 0
6-0	**Reserved**	always reads 0

Offset 8 - Revision ID (nnh)... RO

7-0	**Silicon Revision Code**	default = nnh

Offset 9 - Programming Interface (00h)....................... *RO

Offset A - Sub Class Code (80h).................................... *RO

Offset B - Base Class Code (07h).................................. *RO

*Registers 9-B are RW if function 5-6 Rx44[5] = 1

Offset 13-10 - Base Address 0 – SGD Control / Status .. RW

31-16	**Reserved**	always reads 0
15-8	**Base Address**	default = 00h
7-0	**00000001b (256 bytes)**	

Device 0 Offset 2D-2C – Subsystem Vendor ID (0000h)*RO

15-0	**Subsystem Vendor ID**	default = 0

*This register is RW if function 5-6 Rx44[4] = 1

Device 0 Offset 2F-2E – Subsystem ID (0000h)............. *RO

15-0	**Subsystem ID**	default = 0

*This register is RW if function 5-6 Rx44[4] = 1

Offset 3C - Interrupt Line (00h)..................................... RW

7-4	**Reserved**	always reads 0
3-0	**Modem Interrupt Routing**	
	0000 Disabled	default
	0001 IRQ1	
	0010 Reserved	
	0011 IRQ3	
	0100 IRQ4	
	0101 IRQ5	
	0110 IRQ6	
	0111 IRQ7	
	1000 IRQ8	
	1001 IRQ9	
	1010 IRQ10	
	1011 IRQ11	
	1100 IRQ12	
	1101 IRQ13	
	1110 IRQ14	
	1111 Disabled	
	<u>APIC</u> (See Device 17 Function 0 Rx4D[7])	
	x000 IRQ16	
	x001 IRQ17	
	x010 IRQ18	
	… …	
	x111 IRQ23	

Offset 3D - Interrupt Pin (03h).. RO

Offset 3E - Minimum Grant (00h)................................... RO

Offset 3F - Maximum Latency (00h)................................ RO

Modem-Specific PCI Configuration Registers

Offset 40 – AC Link Interface Status .... RO

- **7-6 Reserved** .... always reads 0
- **5 Codec CID=11b Ready Status............................ RO**
  - 0 Codec Not Ready
  - 1 Codec Ready (modem ctrlr can access codec)
- **4 Codec CID=10b Ready Status............................ RO**
  - 0 Codec Not Ready
  - 1 Codec Ready (modem ctrlr can access codec)
- **3 Reserved** .... always reads 0
- **2 Codec CID=01b Ready Status............................ RO**
  - 0 Codec Not Ready
  - 1 Codec Ready (modem ctrlr can access codec)
- **1 AC97 Low-Power Status .... RO**
  - 0 AC97 Codecs not in low-power mode
  - 1 AC97 Codecs in low-power mode

    This bit reports 1 when Rx26[4] of the codecs is 1. It is used to determine whether the bit-clock should be gated.
- **0 Codec CID=00b Ready Status............................ RO**
  - 0 Codec Not Ready
  - 1 Codec Ready (modem ctrlr can access codec)

Offset 41 – AC Link Interface Control .... RW

- **7 AC-Link Interface**
  - 0 Disable .... default
  - 1 Enable
- **6 AC-Link Reset**

  0Assert AC-Link Reset (used for cold reset).......... def

  1De-assert AC-Link Reset
- **5 AC-Link Sync**
  - 0 Release SYNC .... default
  - 1 Force SYNC High (used for warm reset)
- **4 AC-Link Serial Data Out**
  - 0 Release SDO.. default
  - 1 Force SDO High
- **3 Variable-Sample-Rate On-Demand Mode .... RO**

  This bit is controlled through function 5 but may be read from function 6.
  - 0 Disable (AC Link sends data every frame).. def
  - 1 Enable (AC Link sends data only when there is a request from the codec)
- **2 3D Audio Channel Slots 3/4 .... RO**

  This bit is controlled through function 5 but may be read from function 6.
  - 0 Disable .... default
  - 1 Enable

  Note that slots 7/8 and 6/9 do not have to be selected as they are not muxed with DXS as are slots 3/4)
- **1-0 Reserved** .... always reads 0

Offset 42 – Function Enable .... RO

This register is controlled through function 5 but may be read from function 6.

- **7-6 Reserved** .... always reads 0
- **5 Function 5 Config Reg Rx2C Writable** .... RO
  - 0 Device 17 Function 5 Rx2C-2F RO ...... default
  - 1 Device 17 Function 5 Rx2C-2F RW
- **4-0 Reserved** .... always reads 0

Offset 44 – MC97 Interface Control ....RW

- **7 AC-Link Interface for Slot-5 (Modem)**
  - 0 Disable .... default
  - 1 Enable
- **6 Secondary Codec Support**
  - 0 Disable .... default
  - 1 Enable
- **5 Function 6 Config Reg Rx9-B Writable**
  - 0 Device 17 Function 6 Rx9-B RO .... default
  - 1 Device 17 Function 6 Rx9-B RW
- **4 Function 6 Config Reg 2Ch Writable**
  - 0 Device 17 Function 6 Rx2C-2F RO ...... default
  - 1 Device 17 Function 6 Rx2C-2F RW
- **3 Sync**
  This bit reports whether there is activity in function 6 (modem). When function 5 (audio) enters low-power state and wants to gate bit-clock, software needs to check this bit to see whether bit-clock can actually be gated, as function 6 shares the same bit-clock.
  - 0 Function 6 activity in progress that requires bit-clock
  - 1 Function 6 does not need bit-clock so bit-clock can be gated
- **2-0 Reserved** .... always reads 0

Offset 48 – Volume Change Rate Control ....RO

This register is controlled through function 5 but may be read from function 6.

- **7-4 Volume Change Rate...RO**
  This field controls the volume change rate in the sample rate converter
  - 0000 Volume Adjust Every Frame (sync cycle)...def
  - …
  - 1111 Volume Adjust Every 16 Frames (sync cycles)
- **3 Sync ....RO**
  This bit reports whether there is activity in function 5 (audio). When function 6 (modem) enters low-power state and wants to gate bit-clock, software needs to check this bit to see whether bit-clock can actually be gated, as function 5 shares the same bit-clock.
  - 0 Function 5 activity in progress that requires bit-clock
  - 1 Function 5 does not need bit-clock so bit-clock can be gated
- **2-0 Reserved** .... **RW**

Offset 49 – S/PDIF Control...RO

This register is controlled through function 5 but may be read from function 6.

- **7-4 Reserved** .... **RO**
- **3 DX3 (DirectSound) Channel S/PDIF Support ..RO**
  This bit controls whether DirectSound Channel 3 is used as S/PDIF support
  - 0 Disable .... default
  - 1 Enable
- **2 Reserved** .... **RO**
- **1-0 S/PDIF Data Slot Select......................................RO**
  - 00 Slot 10/11... default
  - 01 Slot 3/4
  - 10 Slot 7/8
  - 11 Slot 6/9

Offset D3-D0 – Power Mgmt Capability.........................RO

- **31-0 Power Mgmt Capability**....always reads 0002 0001h

Offset D7-D4 – Power State .... RW

- **31-2 Reserved** ....always reads 0
- **1-0 Power State (D3 / D0 Only)**

I/O Base 0 Regs – Modem Scatter / Gather DMA

Modem SGD Read Channel Registers

I/O Offset 40 – Modem SGD Read Channel Status.....RWC

- **7 SGD Active** .... **RO**
  - 0 SGD has completed or been terminated default
  - 1 SGD Active
- **6 SGD Paused** .... **RO**
  - 0 SGD not paused.................................... default
  - 1 SGD Paused
- **5-4 Reserved** .... always reads 0
- **3 SGD Trigger Queued** .... **RO**
  This bit reports whether the trigger used to restart the SGD operation is queued (I/O Offset 41[1] = 1 while the SGD engine is running).
  - 0 SGD trigger not queued........................ default
  - 1 SGD trigger queued (when SGD reaches EOL, it will restart).
- **2 SGD Stop Interrupt Status..............................RWC**
  - 1 SGD finished the index equal to the stop index set in 4B-48[31-24].
- **1 SGD EOL (End Of Link).................................RWC**
  - 1 Block is the last of the link. May be used by software as a signal to generate an interrupt request if I/O Offset 41[1] = 1.
- **0 SGD Flag** ....**RWC**
  - 1 Block complete. May be used by software as a signal to generate an interrupt request if I/O Offset 41[0] = 1.

I/O Offset 41 – Modem SGD Read Channel Control.....RW

- **7 SGD Start ....WO (always reads 0)**
  - 0 No effect
  - 1 Start SGD read channel operation
- **6 SGD Terminate ....WO (always reads 0)**
  - 0 No effect
  - 1 Terminate SGD read channel operation
- **5-4 Test (Do Not Program)** ....always write 0
- **3 SGD Pause** ....**RW**
  - 0 Release SGD read channel pause and resume the transfer from the paused line
  - 1 Pause SGD read channel operation (SGD read channel pointer stays at the current address)
- **2-0 Reserved** .... always reads 0

I/O Offset 42 – Modem SGD Read Channel Type .... RW

- **7 Auto-Start SGD at EOL**
  - 0 Stop at EOL .... default
  - 1 Auto restart at EOL
- **6-4 Reserved** ....always reads 0
- **3-2 Interrupt Select**
  This bit determines the timing of interrupt generation when bit-1 or bit-0 of this register are equal to 1.
  - 00 Interrupt at PCI Read of Last Line......... default
  - 01 Interrupt at Last Sample Sent
  - 10 Interrupt at Less Than One Line to Send
  - 11 -reserved-
- **1 Interrupt on EOL @ End of Block**
  - 0 Disable .... default
  - 1 Enable
- **0 Interrupt on FLAG @ End-of-Blk**
  - 0 Disable .... default
  - 1 Enable

I/O Offset 47-44 – Modem SGD R Ch Table Ptr Base... RW

- **31-0 SGD Table Pointer Base Address (even addr) .... W**
  Current Pointer Address .... R

I/O Offset 4F-4C – Modem SGD R Ch Current Count.. RO

- **31-24 Current Modem SGD Read Channel Index**
  This field reports the index the SGD engine is currently processing.
- **23-0 Current Modem SGD Read Channel Count**
  This field reports the count remaining in the current entry being processed. For example, if 10 bytes of a 30-byte count have been transferred, this field would read 20 to indicate 20 bytes remaining.

Modem SGD Table Format

63	62	61	60-56	55-32	31-0
EOL	FLAG	STOP	-reserved-	Base Count [23:0]	Base Address [31:0]

Modem SGD Write Channel Registers

I/O Offset 50 – Modem SGD Write Channel Status....... RO

- **7 SGD Active .... RO**
  - 0 SGD has completed or been terminated default
  - 1 SGD Active
- **6 SGD Paused .... RO**
  - 0 SGD not paused.................................... default
  - 1 SGD Paused
- **5-4 Reserved** .... always reads 0
- **3 SGD Trigger Queued .... RO**
  This bit reports whether the trigger used to restart the SGD operation is queued (I/O Offset 51[1] = 1 while the SGD engine is running).
  - 0 SGD trigger not queued......................... default
  - 1 SGD trigger queued (when SGD reaches EOL, it will restart).
- **2 SGD Stop Interrupt Status..............................RWC**
  - 1 SGD finished the index equal to the stop index set in 5B-58[31-24].
- **1 SGD EOL (End Of Link)................................RWC**
  - 1 Block is the last of the link. May be used by software as a signal to generate an interrupt request if I/O Offset 51[1] = 1.
- **0 SGD Flag ....RWC**
  - 1 Block complete. May be used by software as a signal to generate an interrupt request if I/O Offset 51[0] = 1.

I/O Offset 51 – Modem SGD Write Channel Control....RW

- **7 SGD Start .... WO (always reads 0)**
  - 0 No effect
  - 1 Start SGD write channel operation
- **6 SGD Terminate .... WO (always reads 0)**
  - 0 No effect
  - 1 Terminate SGD write channel operation
- **5-4 Test (Do Not Program)** ....always write 0
- **3 SGD Pause ....RW**
  - 0 Release SGD write channel pause and resume the transfer from the paused line
  - 1 Pause SGD write channel operation (SGD write channel pointer stays at current address)
- **2 Reserved** .... always reads 0
- **1 Reset Modem Write SGD Operation.................RW**
- **0 Reserved** .... always reads 0

I/O Offset 52 – Modem SGD Write Channel Type .... RW

- **7 Auto-Start SGD at EOL**
  - 0 Stop at EOL .... default
  - 1 Auto restart at EOL
- **6-2 Reserved** ....always reads 0
- **1 Interrupt on EOL @ End of Block**
  - 0 Disable .... default
  - 1 Enable
- **0 Interrupt on FLAG @ End-of-Blk**
  - 0 Disable .... default
  - 1 Enable

I/O Offset 57-54 – Modem SGD W Ch Table Ptr Base . RW

- **31-0 SGD Table Pointer Base Address (even addr) .... W**
  Current Pointer Address .... R

I/O Offset 5F-5C – Modem SGD W Ch Current Count. RO

- **31-24 Current Modem SGD Write Channel Index**
  This field reports the index the SGD engine is currently processing.
- **23-0 Current Modem SGD Write Channel Count**
  This field reports the count remaining in the current entry being processed. For example, if 10 bytes of a 30-byte count have been transferred, this field would read 20 to indicate 20 bytes remaining.

EOL End Of Link. 1 indicates this block is the last of the link. If the channel "Interrupt on EOL" bit is set, then an interrupt is generated at the end of the transfer.

FLAG Block Flag. If set, transfer pauses at the end of this block. If the channel "Interrupt on FLAG" bit is set, then an interrupt is generated at the end of this block.

STOP Block Stop. If set, transfer pauses at the end of this block. To resume the transfer, write 1 to Rx?0[2].

Codec Command / Status SGD Registers

These registers are used to send commands to the codecs

Offset 83-80 – AC97 Controller Command (W) / Status (R)

This register may be accessed from either function 5 or 6

31-30 Codec ID .... RW
- 00 Select Codec CID = 00
- 01 Select Codec CID = 01
- 10 Select Codec CID = 10
- 11 Select Codec CID = 11

29 Codec 11 Data / Status / Index Valid .... RO
- 0 Not Valid
- 1 Valid (OK to Read bits 0-23)

28 Codec 10 Data / Status / Index Valid .... RO
- 0 Not Valid
- 1 Valid (OK to Read bits 0-23)

27 Codec 01 Data / Status / Index Valid .... RO
- 0 Not Valid
- 1 Valid (OK to Read bits 0-23)

26 Reserved .... always reads 0

25 Codec 00 Data / Status / Index Valid .... RO
- 0 Not Valid
- 1 Valid (OK to Read bits 0-23)

24 AC97 Controller Busy .... RO
- 0 Codec is ready for a register access command
- 1 AC97 Controller is sending a command to the codec (commands are not accepted)

23 Codec Register Read / Write Mode .... RW
- 0 Select Codec register write mode
- 1 Select Codec register read mode

22-16 Codec Register Index [7:1] .... RW
Index of the AC97 codec register to access (in the attached codec). Data must be written before or at the same time as Index because writing to the index triggers the AC97 controller to access the addressed codec register over the AC-link interface.

15-0 Codec Register Data .... RW

Offset 87-84 – Modem SGD Status Shadow .... RO

31-30 Reserved .... always reads 0
29 Modem Write SGD Active Shadow .... **(Rx50[7])**
28 Modem Read SGD Active Shadow .... **(Rx40[7])**
27-26 Reserved .... always reads 0
25 Modem Write SGD Stop Shadow .... **(Rx50[2])**
24 Modem Read SGD Stop Shadow .... **(Rx40[2])**

23-22 Reserved .... always reads 0
21 Modem Write SGD EOL Shadow .... **(Rx50[1])**
20 Modem Read SGD EOL Shadow .... **(Rx40[1])**
19-18 Reserved .... always reads 0
17 Modem Write SGD Flag Shadow .... **(Rx50[0])**
16 Modem Read SGD Flag Shadow .... **(Rx40[0])**

15-0 Reserved .... always reads 0

Offset 8B-88 – Codec GPI Interrupt Status / GPIO ... RWC

This register may be accessed from either function 5 or 6

31-16 GPI Interrupt Status .... RWC
- R GPI[15-0] Interrupt Status
- W 1 to clear

15-0 Codec GPIO .... RW
- R Reflect status of Codec GPI[15-0]
- W Triggers AC-Link slot-12 output to codec

Offset 8F-8C – Codec GPI Interrupt Enable .... RW

This register may be accessed from either function 5 or 6

31-16 Interrupt on GPI[15-0] Change of Status .... RW
- 0 Disable
- 1 Enable

15-0 Reserved .... always reads 0

Offset 90-9F – Mapped from Function 5/6 Rx40-4F .... RO

Device 18 Function 0 Registers - LAN

All registers are located in the Device 18 Function 0 PCI configuration space of the VT8235. These registers are accessed through PCI configuration mechanism #1 via I/O address CF8 / CFC.

PCI Configuration Space Header

Offset 1-0 - Vendor ID = 1106h .... RO

Offset 3-2 - Device ID = 3065h... RO

Offset 5-4 - Command...RW

15-3	**Reserved**	always reads 0
2	**Bus Master**	always reads 0
1	**Memory Space**	always reads 0
0	**I/O Space**	RW, default = 0

Offset 7-6 – Status (0400h)... RO

15	**Detected Parity Error**	always reads 0
14	**Signalled System Error**	always reads 0
13	**Received Master Abort**	always reads 0
12	**Received Target Abort**	always reads 0
11	**Signalled Target Abort**	always reads 0
10-9	**DEVSEL# Timing**	fixed at 10 (slow)
8	**Data Parity Detected**	always reads 0
7	**Fast Back-to-Back Capable**	always reads 0
6	**UDF Support**	always reads 1
5	**66 MHz Capable**	always reads 1
4	**Capabilities (e.g. PCI Pwr Mgmt)**	always reads 1
3-0	**Reserved**	always reads 0

Offset 8 - Revision ID (40h) .... RO

Offset 9 - Program Interface .... RO

Offset A - Sub Class Code... RO

Offset B - Class Code .... RO

Offset C – Cache Line Size ....RW

This register must be implemented by master devices that can generate the memory-write-and-invalidate command.

Offset D – Latency Timer ....RW

This register must be implemented as writable by any master that can burst more than two data phases.

Offset E - Header Type (00h) .... RO

Offset F - BIST (00h)... RO

Offset 13-10 – I/O Base Address (0000 0000h)................RW

Offset 17-14 – Memory Base Address (0000 0000h).......RW

Offset 2B-28 – Card Bus CIS Pointer (0000 0000h) ....RW

Offset 33-30 – Expansion ROM Base (0000 0000h)........RW

Offset 34 – Capabilities Offset (40h) ....RO

7-0 Capabilities Offset
Offset into the LAN function PCI space pointing to the location of the first item in the function's capability list.

Offset 3C - Interrupt Line..RW

7-4 Reserved ....always reads 0

3-0 LAN Interrupt Routing

0000	Disabled .... default
0001	IRQ1
0010	Reserved
0011	IRQ3
0100	IRQ4
0101	IRQ5
0110	IRQ6
0111	IRQ7
1000	IRQ8
1001	IRQ9
1010	IRQ10
1011	IRQ11
1100	IRQ12
1101	IRQ13
1110	IRQ14
1111	Disabled

APIC (See Device 17 Function 0 Rx4D[7])

x000	IRQ16
x001	IRQ17
x010	IRQ18
…	…
x111	IRQ23

Offset 3D - Interrupt Pin (01h)...RO

7-0 Interrupt Routing Mode

00h	Legacy mode interrupt routing
01h	Native mode interrupt routing .... default

LAN-Specific PCI Configuration Registers

Offset 40 – Capability ID (01h)..RO

7-0 Capability ID ....always reads 01h
Identifies the linked list item as being PCI power management registers

Offset 41 – Next Item Pointer (00h).................................RO

7-0 Next Item Pointer ....always reads 00h
Offset into the LAN function PCI space pointing to the location of the next item in the function's capability list.

Offset 43-42 – Power Mgmt Configuration (0002h) .... RO

15-11 Power State In Which LAN Can Assert PME# .... default = 0
- **1xxxx PME# can be asserted from D3C**
- **x1xxx PME# can be asserted from D3H**
- **xx1xx PME# can be asserted from D2**
- **xxx1x PME# can be asserted from D1**
- **xxxx1 PME# can be asserted from D0**

10 D2 PM State
- 0 Not Supported .... default
- 1 Supported

9 D1 PM State
- 0 Not Supported .... default
- 1 Supported

8-6 PCI 3.3V Auxiliary Current Requirements .... always reads 0

5 Device-Specific Initialization .... always reads 0

4 Reserved .... always reads 0

3 PME# Operation Uses PCI Clock
- 0 No PCI clock req'd for PME# generation ... def
- 1 PME# generated using PCI clock

2-0 Power Management Interface Revision . reads 010b
Readback of 010b indicates compliance with revision 1.1 of the power mangement interface specification

Offset 47-44 – Power Management Control / Status... RWC

31-0 Control / Status .... default = 0000 0000h
(see Power Management Specification 1.0)

LAN I/O Registers

Offset 05-00 – Ethernet Address ....RW

Unless the EEPROM is disabled, the Ethernet Address is loaded to this register from the EEPROM every time the system starts up.

Offset 06 – Receive Control (00h) ....RW

7-5 Receive FIFO Threshold
This field determines the threshold required before data in the receive FIFO is forwarded. When the FIFO reaches the level selected in this field, data will start being forwarded.
- 000 64 byte .... default
- 001 32 byte
- 010 128 byte
- 011 256 byte
- 100 512 byte
- 101 768 byte
- 110 1024 byte
- 111 Store & Forward (data is forwarded after the entire packet has been received)

4 Physical Address Packets Accepted
- 0 Packets with a physical destination address are not accepted.. default
- 1 All packets with a physical destination address are accepted.. default

3 Broadcast Packets Accepted
- 0 Broadcast packets are rejected .... default
- 1 Broadcast packets are accepted

2 Multicast Packets Accepted
- 0 Multicast packets are rejected .... default
- 1 Multicast packets are accepted

1 Small Packets Accepted
- 0 Packets smaller than 64 bytes are rejected .. def
- 1 Packets smaller than 64 bytes are accepted

0 Error Packets Accepted
- 0 Packets with receive errors are rejected ...... def
- 1 Packets with receive errors are accepted

Offset 07 – Transmit Control (08h)................................ RW

7-5 Transmit FIFO Threshold
This field determines the threshold required before data in the transmit FIFO is forwarded. When the FIFO reaches the level selected in this field, data will start being forwarded.

	100T	10T	
000	128 byte	64 byte	.... default
001	256 byte	128 byte	
010	512 byte	256 byte	
011	1024 byte	512 byte	
1xx	Store & Forward		

4 Reserved .... always reads 0

3 Backoff Priority Selection
This bit determines the backoff algorithm used when collision occurs.
- 0 VIA backoff algorithm
- 1 NSC compatible backoff algorithm ...... **default**

2-1 Transmit Loopback Mode
- 00 Normal.. default
- 01 Internal loopback (signal is looped back to the host from the MAC)
- 10 MII loopback (signal is looped back to the host from the PHY)
- 11 -reserved- (do not program)

0 Reserved .... always reads 0

Offset 08 – Command 0 (00h)..RW

- **7 Reserved** .... always reads 0
- **6 Receive Poll Demand** .... default = 0
  If this bit is set to 1, the Receive Descriptor (RD) will be polled once (this bit will be cleared by hardware after the polling is complete)
- **5 Transmit Poll Demand**............................. default = 0
  If this bit is set to 1, the Transmit Descriptor (TD) will be polled once (this bit will be cleared by hardware after the polling is complete)
- **4 Transmit Process**
  - 0 Transmit engine disabled....................... default
  - 1 Transmit engine enabled (transmit may occur)
- **3 Receive Process**
  - 0 Receive disabled.................................... default
  - 1 Receive enabled
- **2 Stop NIC**
  - 0 NIC enabled .... default
  - 1 NIC disabled (transmit/receive cannot occur)
- **1 Start NIC**
  - 0 No command entered .... default
  - 1 Start the NIC
- **0 Begin Initialization Process** .... default = 0
  If this bit is set to 1, the Receive Descriptor (RD) will be polled once (this bit functions like bit-6 but for legacy systems)

Offset 09 – Command 1 (00h)...RW

- **7 Software Reset**
  - 0 No reset.. default
  - 1 Reset the MAC
- **6 Receive Poll Demand 1** ....default = 0
  This bit functions the same as Rx8[6]. The function can be enabled by setting either bit (for backward compatibility).
- **5 Transmit Poll Demand 1** ....default = 0
  This bit functions the same as Rx8[5]. The function can be enabled by setting either bit (for backward compatibility).
- **4 Reserved** ....always reads 0
- **3 TD / RD Auto Polling**
  - 0 Enable (polling interval is determined by Rx6F[2:0]) .... default
  - 1 Disable
- **2 Full Duplex**
  - 0 Set MAC to half duplex mode .... default
  - 1 Set MAC to full duplex mode
- **1 Reserved** ....always reads 0
- **0 Early Receive Mode**
  - 0 Disable (interrupt is generated after a packet has been completely received)............... default
  - 1 Enable (interrupt is generated as soon as packet reception has started)

Offset 0C – Interrupt Status 0 (00h)................................RW

- **7 CRC or Miss Packet Tally Counter Overflow**
  Set if either counter overflows (both counters are 16 bits)
- **6 PCI Bus Error**
  Set if PCI bus error occurred.
- **5 Receive Buffer Link Error**
  Set when there is not enough buffer space for a packet requiring multiple buffers.
- **4 Transmit Buffer Underflow**
- **3 Transmit Error (Packet Transmit Aborted)**
  Set due to excessive collisions (more than 16), transmit underflow, or transmit data linking error
- **2 Receive Error**
  Set due to CRC error, frame alignment error, FIFO overflow, or received data linking error
- **1 Packet Transmitted Successfully**
- **0 Packet Received Successfully**

Offset 0D – Interrupt Status 1 (00h)................................RW

- **7 General Purpose Interrupt**
  This bit is set when there is a general purpose interrupt event (Rx84). This bit is set when any bit in Rx84 equals one and when its corresponding mask bit in Rx86 also equals one.
- **6 Port State Change (PHY)**
- **5 Transmit Abort Due to Excessive Collisions**
  Set when there is a transmit error that is due to excessive collisions. Alternatively, Rx0C[3] is set for all transmit errors.
- **4 Receive Buffer Full**
  Set when there is no more buffer space available in system memory.
- **3 Receive Packet Race**
  Set when there is not enough room in the FIFO to receive an additional packet.
- **2 Receive FIFO Overflow**
- **1 Transmit FIFO Underflow**
- **0 Early Receive Interrupt**
  Set if a packet is being received and Rx9[0] = 1.

Offset 0E – Interrupt Mask 0 (00h)................................RW

Bits correspond to the bits in Interrupt Status Register 0. An interrupt is generated when corresponding bits in both registers equal 1.

Offset 0F – Interrupt Mask 1 (00h)................................RW

Bits correspond to the bits in Interrupt Status Register 1. An interrupt is generated when corresponding bits in both registers equal 1.

Offset 17-10 – Multicast Address....................................RW

The value in this register determines which Multicast addresses are received.

Offset 1B-18 – RX Address ....RW

This register reports the receive transcriptor address that is being accessed.

Offset 1F-1C – TX Address...RW

This register reports the transmit transcriptor address that is being accessed.

Offset 23-20 – Receive Status (0000 0000h)......................RW

31 Descriptor Owner
- 0 Descriptor Owned By Host (NIC cannot access descriptor)
- 1 Descriptor Owned by NIC (NIC can access descriptor)

This bit has no default so must be set by the driver at initialization.

30-27 Reserved .... always reads 0
26-16 Received Packet Length......................... **RO,** def = 0
15 Received Packet Successfully .... **RO,** def = 0
14 Reserved .... always reads 0
13 NIC Accepted Multicast Packet .... **RO,** def = 0
12 NIC Accepted Broadcast Packet .... **RO,** def = 0
11 NIC Accepted Physical Address PacketRO, def = 0
10 Chain Buffer .... def = 0
Set if packet too large to occupy a single receive transcriptor.
9-8 Buffer Descriptor Start / End............................ **RO**
For packets too large to fit into a single receive descriptor and thus occupy multiple RD's, this field reports whether this RD is the start, middle or end.
- 00 Chain Buffer Middle Descriptor............ default
- 01 Chain Buffer End Descriptor
- 10 Chain Buffer Start Descriptor
- 11 Single Buffer Descriptor (packet accupies only one descriptor)

7 Buffer Underflow Error .... **RO,** default = 0
6 System Error .... **RO,** default = 0
5 Run Packet (< 64 bytes) .... **RO,** default = 0
4 Long Packet (> 2500 bytes).............. **RO,** default = 0
3 FIFO Overflow Error .... **RO,** default = 0
2 Frame Alignment Error .... **RO,** default = 0
1 CRC Error .... **RO,** default = 0
0 Receiver Error................................. **RO,** default = 0

Offset 27-24 – Rx Data Buffer Control (0000 0000h)..... RO

31-11 Reserved .... always reads 0
10-0 Rx Data Buffer Size.................................. default = 0
The receive data buffer size for this descriptor. The total byte count of the entire frame will be stored in the last descriptor.

Offset 2B-28 – Rx Data Buffer Start Address .... RO

31-0 Rx Data Buffer Start Address

Offset 2F-2C – Rx Data Buffer Branch Address............. RO

31-0 Rx Data Buffer Branch Address

Note: Rx20-2F reflect values from the RD being accessed.

Offset 43-40 – Transmit Status (0000 0000h)..................RW

31 Descriptor Owner
- 0 Descriptor Owned By Host (NIC cannot access descriptor)
- 1 Descriptor Owned by NIC (NIC can access descriptor)

This bit has no default so must be set by the driver at initialization.

30-16 Reserved .... always reads 0

15 Transmit Error................................. **RO,** default = 0
- 0 Transmit Successful .... default
- 1 Excessive Collisions During Transmit Attempt

14 Reserved .... always reads 0

13 System Error .... **RO,** default = 0

12 Invalid TD Format or Structure or TD Overflow .... **RO,** default = 0

11 Transmit Data FIFO Underflow........... **RO,** def = 0

10 Carrier Sense Lost During Transmit ... **RO,** def = 0

9 Out of Window Collision .... **RO,** def = 0
(collision outside initial 64 bytes)

8 Transmit Abort (Excessive Collisions) . **RO,** def = 0

7 CD Heartbeat Issued (10BaseT Only) ... **RO,** def = 0

6-5 Reserved .... always reads 0

4 Collision Detected During Transmit..... **RO,** def = 0

3-0 Collision Retry Count .... **RO,** def = 0

Offset 47-44 – Tx Data Buffer Control (0000 0000h)...... RO

31-24 Reserved .... always reads 0

23 Send-Complete Interrupt
- 0 Interrupt not generated........................... default
- 1 Interrupt generated after send complete

22 End of Transmit Packet
For packets too large to fit into a single transmit descriptor and thus occupy multiple TD's, this bit reports whether this TD is the End TD.
- 0 This TD is not the End TD .... default
- 1 This TD is the End TD

21 Start of Transmit Packet
For packets too large to fit into a single transmit descriptor and thus occupy multiple TD's, this bit reports whether this TD is the Start TD.
- 0 This TD is not the Start TD .... default
- 1 This TD is the Start TD

20-17 Reserved .... always reads 0

16 Disable CRC Generation .... default = 0

15 Chain Buffer .... default = 0

14-11 Reserved .... always reads 0

10-0 Tx Data Buffer Size .... default = 0
The transmit data buffer size for this descriptor. The total byte count of the entire frame will be stored in the last descriptor.

Offset 4B-48 – Tx Data Buffer Start Address.................. RO

31-0 Tx Data Buffer Start Address

Offset 4F-4C – Tx Data Buffer Branch Address............. RO

31-4 Tx Data Buffer Branch Address

3-1 Reserved .... always reads 0

0 Tx Interrupt Enable
- 0 Issue interrupt for this packet................. default
- 1 No interrupt generated

Offset 6C – PHY Address (01h) ....RW

7-6 MII Management Polling Timer Interval (Polling PHY)
- 00 1024 MDC Clock Cycles .... default
- 01 512 MDC Clock Cycles
- 10 128 MDC Clock Cycles
- 11 64 MDC Clock Cycles

MDC is an internal clock with a 960 ns cycle time.

5 Accelerate MDC Speed
- 0 Normal .... default
- 1 4x Accelerated

4-0 Extended PHY Device Address.......... default = 01h
Stored from EEPROM during power-up or EEPROM auto-reload but can be programmed by software

Offset 6D – MII Status (13h) ....RW

7 PHY Reset
- 0 PHY reset not asserted .... default
- 1 PHY reset asserted

6-5 Reserved .... always reads 0

4 PHY Option
- 0 PHY address updated from EEPROM
- 1 Use default PHY address of 0001h **.......default**

3 PHY Device Received Error
- 0 No MII error... default
- 1 MII Error

2 Reserved .... always reads 0

1 Link Failure
- 0 Link successful
- 1 Link unsuccessful (no connection)**........default**

0 PHY Speed
- 0 100 Mb
- 1 10 Mb **...default**

Offset 6E – Buffer Control 0 (00h)................................. RW

7-6 Reserved ....always reads 0

5-3 Rx FIFO Threshold Control
- 000 Determined by Offset 6 Rcv Ctrl Reg.... default
- ~000 Determined by bits 2-0 of this register

2-0 DMA Length

000	32 bytes	8 DW .... default
001	64 bytes	16 DW
010	128 bytes	32 DW
011	256 bytes	64 DW
100	512 bytes	128 DW
101	1024 bytes	256 DW
11x	Store & Forward	

Offset 6F – Buffer Control 1 (00h) .... RW

7-6 Reserved ....always reads 0

5-3 Tx FIFO Threshold Control
- 000 Determined by Rx7 Transmit Control ... default
- ~000 Determined by this register

2-0 Polling Interval Timer
This field determines the polling interval when TD / RD Auto-Polling is enabled (Rx09[3]=0).
- 000 4 PCI Clocks... default
- 001 1 PCI Clock
- 010 2 PCI Clocks
- 011 8 PCI Clocks
- 100 16 PCI Clocks
- 101 32 PCI Clocks
- 110 64 PCI Clocks
- 111 128 PCI Clocks

Offset 70 – MII Management Port Command (00h) ......RW

7 MII (PHY) Auto Polling
- 0 Disable .... default
- 1 Enable (polling interval determined by Rx6C[7:6])

6 PHY Read
Every time this bit is set to one, the PHY is read once. The address read is determined by Rx71[4:0] and the data is stored in Rx73-72.

5 PHY Write
Every time this bit is set to one, the PHY is written once. The address written is determined by Rx71[4:0] and the value in Rx73-72 will be written to the PHY.
- 0 Disable .... default
- 1 Enable

4 PHY Direct Programming Mode
- 0 Disable (bits 3-0 are ignored) (see bits 6-5) def
- 1 Enable (bits 6-5 are ignored) (see bits 2-0)

3 MDIO Output Enable Indicator

2 PHY Direct Programming Write Data Out
During direct programming (write), the value in this bit is written to the PHY every time bit-0 of this register (the "clock") toggles.

1 PHY Direct Programming Read Data In .... RO
During direct programming (read), every time the "clock" (bit-0) toggles, the value from the PHY is stored in this bit.

0 PHY Direct Programming Clock
This bit acts as the clock during direct reads from and direct writes to the PHY.

Offset 71 – MII Management Port Address (81h) ....RW

7 Polling Status
- 0 Polling mechanism is busy (polling can't be initiated)
- 1 Polling mechanism is idle (polling can be initiated) **...default**

6 Polling Type
- 0 Poll One Cycle .... default
- 1 Auto polling – close the pause function at bit-5

5 Polling Complete
- 0 Polling not complete............................. default
- 1 Polling complete (auto polling data ready)

4-0 MII Management Port Address Bits 4-0 ..def = 01h
This field contains the address of the PHY register to be read or written.

Offset 73-72 – PHY Data...RW

After a PHY read, the data read from the PHY is stored in this register. For writes to the PHY, the data to be written is placed in this register.

Offset 74 – EEPROM Command / Status (00h) .... RW

7 EEPROM Program Complete...............RO, def = 0
Set when EEPROM loading is complete.

6 EEPROM Embedded Program Enable........def = 0
When this bit is set, configuration data (in Rx6E, 6F, 74, 78, 79, 7A, and 7B) will start to be programmed into the EEPROM.

5 Dynamically Reload EEPROM Content ......def = 0
When this bit toggles, the Ethernet ID (Rx5-0) is reloaded from EEPROM.

4 EEPROM Direct Program Mode
- 0 Disable .... default
- 1 Enable (see bits 3-0)

3 EEPROM Direct Programming Chip Select
This bit must be set to allow proramming of the EEPROM using bits 2-0

2 EEPROM Direct Programming Clock
This bit acts as the clock for direct programming of the EEPROM.

1 EEPROM Direct Programming Read Data In . RO
During direct programming (read), the value in this bit is written to the EEPROM every time bit-2 of this register (the "clock") toggles.

0 EEPROM Direct Programming Wr Data Out
During direct programming (write), the value in this bit is written to the EEPROM every time bit-2 of this register (the "clock") toggles.

Offset 78 – EEPROM Control (00h) .... RW

7 EEPROM Embedded & Direct Programming
- 0 Disable (EEPROM cannot be programmed) def
- 1 Enable (allow EEPROM to be programmed)

6 Extension Clock
- 0 Disable .... default
- 1 Enable (the clock to the EEPROM is sent prior to the start of data to allow more time for the EEPROM to return to the ready state)

5-0 Reserved .... always reads 0

Offset 79 – Configuration 1 (00h)....................................RW

7 Transmit Frame Queueing
- 0 Enable (frames from the PCI bus can be queued in the transmit FIFO – a maximum of 2 packets may be queued) .... default
- 1 Disable

6 Data Parity Generation and Checking
This bit controls whether PCI parity is enabled.
- 0 Enable.. default
- 1 Disable

5 Memory-Read-Line Supported
This bit controls whether PCI Memory-Read-Line is supported.
- 0 Enable.. default
- 1 Disable

4 Transmit FIFO DMA Interleaved to Receiving FIFO DMA After 32 DW Transaction
This bit controls whether during a transmit, priority can be given to a receive transaction.
- 0 Disable .... default
- 1 Enable (during a transmit, if a receive request is seen, the transmit is paused after 32 DW's and priority is given to the receive)

3 Receive FIFO DMA Interleaved to Transmitting FIFO DMA After 32 DW Transaction
This bit controls whether during a receive, priority can be given to a transmit transaction.
- 0 Disable .... default
- 1 Enable (during a receive, if a transmit request is seen, the receive is paused after 32 DW's and priority is given to the transmit)

2 Memory Read Wait States (for ISA only)
- 0 None .... default
- 1 Insert one wait state 2222

1 Memory Write Wait States s (for ISA only)
- 0 None .... default
- 1 Insert one wait state 2222

0 Latency Timer
This bit controls whether PCI Delayed Transactions are enabled.
- 0 Disable .... default
- 1 Enable

Offset 7A – Configuration 2 (00h).................................. RW

7 Reserved .... always reads 0

6 Unused BootROM Address MA
This bit controls whether unused BootROM memory address bits are tied high.
- 0 Not tied high .... default
- 1 Tied high

5 Delayed Transactions for BootROM Memory Read
This bit controls whether PCI delayed transactions are enabled.
- 0 Disable .... default
- 1 Enable

4-0 Reserved .... always reads 0

Offset 7B – Configuration 3 (00h) .... RW

7 Memory Mapped I/O Access
- 0 Disable .... default
- 1 Enable

6-4 Reserved (Do Not Program) .... default = 0

3 Backoff Algorithm
- 0 Fixed .... default
- 1 Random

2 DEC Capture Effect Solution
- 0 Disable .... default
- 1 Enable

1 AMD Capture Effect Solution
- 0 Disable .... default
- 1 Enable

0 Backoff Algorithm Optional
- 0 Disable .... default
- 1 Enable

Offset 80 – Miscellaneous 1 (00h)......................................RW

7-4 Reserved .... always reads 0

3 Full Duplex Flow Control
- 0 Disable .... default
- 1 Enable

2 Half Duplex Flow Control
- 0 Disable .... default
- 1 Enable

1 Soft Timer 0 Status / Start
- 0 Timer Counting .... default (write 0 after time out to start timer counting)
- 1 Timer Timed Out

0 Soft Timer 0 Enable
- 0 Disable .... default
- 1 Enable timer to count

Offset 81 – Miscellaneous 2 (00h)......................................RW

7 Reserved .... always reads 0

6 Force Software Reset
Setting this bit resets the MAC. This bit functions differently from Rx09[7] in that when Rx09[7] is set, the MAC will reset only after all state machines are in idle mode (all on-going transactions have been completed). When this bit is set, the MAC will be reset regardless of the status of the state machines. This bit is used when Rx09[7] cannot force a reset due to issues with the state machines.
- 0 Normal .... default
- 1 Force Reset

5 Reserved (Do Not Program).................... default = 0

4-1 Reserved .... always reads 0

0 Soft Timer 1 Enable
- 0 Disable .... default
- 1 Enable timer to count

Offset 83 – Sticky Hardware Control (00h).................... RW

7 Legacy WOL Status (for software reference) ... RO
This bit reports whether legacy WOL is supported. The value is usually derived from a jumper switch.
- 0 Disable .... default
- 1 Enable

6-4 Reserved .... always reads 0

3 Legacy WOL Status .... RO
This bit is set when there is a legacy WOL event.
- 0 No legacy WOL event occurred .... default
- 1 Legacy WOL event occurred

2 Legacy WOL Enable
This bit controls whether legacy WOL is a wake event.
- 0 Disable (if a wake event is detected (bit-3 = 1), PME# will not be asserted).................... default
- 1 Enable (if a wake event is detected (bit-3 = 1), PME# will be asserted)

1-0 Sticky DS Shadow
This field reports the current power management state of the device.
- 00 D0 State .... default
- 01 D1 State
- 10 D2 State
- 11 D3 State

Offset 84 – MII Interrupt Status (00h)........................RWC

The bits in this register correspond to bits in the MII Interrupt Mask register (Rx86). An interrupt is generated when corresponding bits in both registers equal one.

- **7-4 Reserved (Do Not Program)**.................... default = 0
- **3 Transmit Data Write Buffer Queue Race**.... def = 0
  Set when write back race for transmit occurs. Write back race occurs when a new write back is generated with 2 write backs already queued.
- **2 Reserved** .... always reads 0
- **1 Soft Timer 1 Timeout**............................... default = 0
- **0 Soft Timer 0 Timeout**............................... default = 0
  All bits above: write 0 to clear the interrupt

Offset 86 – MII Interrupt Mask (00h)............................RW

The bits in this register correspond to bits in the MII Interrupt Status register (Rx84). An interrupt is generated when corresponding bits in both registers equal one.

- **7-4 Reserved (Do Not Program)**.................... default = 0
- **3 Transmit Shutdown Interrupt Mask**
- **2 Reserved** .... always reads 0
- **1 Soft Timer 1 Interrupt Mask**
- **0 Soft Timer 0 Interrupt Mask**
  All bits above:
  - 0 Disable .... default
  - 1 Enable

Offset 8D-8C – Flash Address... RW

This register stores the address that is read from or written to when reading or configuring the BootROM.

- **15-0 Flash Address [15:0]**................................default = 0

Offset 8F – Flash Write Data Out .... RW

This register stores the data that is written to the BootROM.

- **7-0 Flash Write Data Out**..............................default = 0

Offset 90 – Flash Read / Write Command...................... RW

- **7-2 Reserved** ....always reads 0
- **1 Boot ROM Embedded Write Command**......def = 0
  Setting this bit initiates a write transaction (data in Rx8F will be written to the address specified in Rx8D-8C).
- **0 Boot ROM Embedded Read Command**.......def = 0
  Setting this bit initiates a read transaction (data in the address specified in Rx8D-8C will be read and stored in Rx91).

Offset 91 – Flash Write Data In....................................... RO

This register stores the data that is read from the BootROM.

- **7-0 Flash Write Data In**.................................default = 0

Offset 93 – Flash Checksum (00h).................................. RW

This register stores the checksum from the BootROM after programming.

- **7-0 EEPROM Checksum** ....default = 0

Offset 95-94 – Suspend Mode MII Address (0000h).......RW

15-0 MII Address During Suspend .... default = 0
Functionally, this field is the same as Rx71[4:0]. However, during suspend state this field is used because Rx71[4:0] cannot be accessed.

Offset 96 – Suspend Mode PHY Address (00h) ....RW

7-0 PHY Address During Suspend................ default = 0
This field stores the address of the PHY to access during suspend state. This field selects the PHY while Rx95-94 selects the specific register within the PHY.

Offset 99-98 – Pause Timer (0000h) .... RW

7-0 Pause Timer Value ....def = 0
This field is used for full duplex flow control. When the Receive FIFO is nearly full, The transmitter can send a pause frame to the transmitting side (generally a switch) to request a pause. The length of pause time is determined by this field.

Offset 9A – Pause Status (00h)... RW

7-1 Reserved ....always reads 0

0 Pause Status
- 0 Not paused .... default
- 1 Paused

Offset 9D-9C – Soft Timer 0 (0000h)............................... RW

7-0 Soft Timer 0 Count Value........................default = 0
This field reports the count value of soft timer 0.

Offset 9F-9E – Soft Timer 1 (0000h) .... RW

7-0 Soft Timer 1 Count Value........................default = 0
This field reports the count value of soft timer 1.

Offset A0 – Wake On LAN Control Set (00h)................RW

Offset A4 – Wake On LAN Control Clear (00h) ....RW

- **7 Link Off Detected** (determines whether the system wakes up from link off detection)
- **6 Link On Detected** (determines whether the system wakes up from link on detection)
- **5 Magic Packet Filter** (determines whether the system wakes up when a Magic Packet is detected)
- **4 Unicast Filter** (determines whether the system wakes up when a Unicast Packet is detected)
- **3 CRC3 Pattern Match Filtering** (determines whether the system wakes up when packet matching CRC3 pattern is detected)
- **2 CRC2 Pattern Match Filtering** (determines whether the system wakes up when packet matching CRC2 pattern is detected)
- **1 CRC1 Pattern Match Filtering** (determines whether the system wakes up when packet matching CRC1 pattern is detected)
- **0 CRC0 Pattern Match Filtering** (determines whether the system wakes up when packet matching CRC0 pattern is detected)

  All bits above:
  - 0 Disable .... default
  - 1 Enable

Offset A1 – Power Configuration Set (00h)....................RW

Offset A5 – Power Configuration Clear (00h) ....RW

- **7-6 Reserved** .... always reads 0
- **5 WOL Type**
  - 0 Driven by Level.................................... default
  - 1 Driven By Pulse
- **4 Legacy WOL**
  - 0 Disable .... default
  - 1 Enable
- **3-2 Reserved** .... always reads 0
- **1-0 Reserved (Do Not Program)**.................... default = 0

Offset A3 – Wake On LAN Configuration Set (00h) ..... RW

Offset A7 – Wake On LAN Configuration Clear (00h). RW

- **7 Force Power Management Enable over PME Enable Bit (Legacy Use Only)**
- **6 Full Duplex During Suspend**
- **5 Accept Multicast During Suspend**

  This bit controls whether multicast packets are accepted during suspend state. Whether a multicast packet will actually wake up the system depends on whether the packet is a type of packet set to wake up the system, as determined by RxA0[5:0].
- **4 Accept Broadcast During Suspend**

  This bit controls whether broadcast packets are accepted during suspend state. Whether a broadcast packet will actually wake up the system depends on whether the packet is a type of packet set to wake up the system, as determined by RxA0[5:0].
- **3 MDC Acceleration**
- **2 Extend Clock During Suspend**

  When enabled, the clock to the PHY is sent prior to the start of data to allow more time for the PHY to return to ready state.
- **1-0 Reserved** .... always reads 0

  All bits above:
  - 0 Disable .... default
  - 1 Enable

Offset B3-B0 – Pattern CRC0.. RW

- **127-0 CRC0 Pattern** ....default = 0

Offset B7-B4 – Pattern CRC1.. RW

- **127-0 CRC1 Pattern** ....default = 0

Offset BB-B8 – Pattern CRC2 .... RW

- **127-0 CRC2 Pattern** ....default = 0

Offset BF-BC – Pattern CRC3 .... RW

- **127-0 CRC3 Pattern** ....default = 0

Offset CF-C0 – Byte Mask 0 .... RW

Offset DF-D0 – Byte Mask 1 .... RW

Offset EF-E0 – Byte Mask 2... RW

Offset FF-F0 – Byte Mask 3 .... RW

FUNCTIONAL DESCRIPTIONS

Power Management

Power Management Subsystem Overview

The power management function of the VT8235 is indicated in the following block diagram:

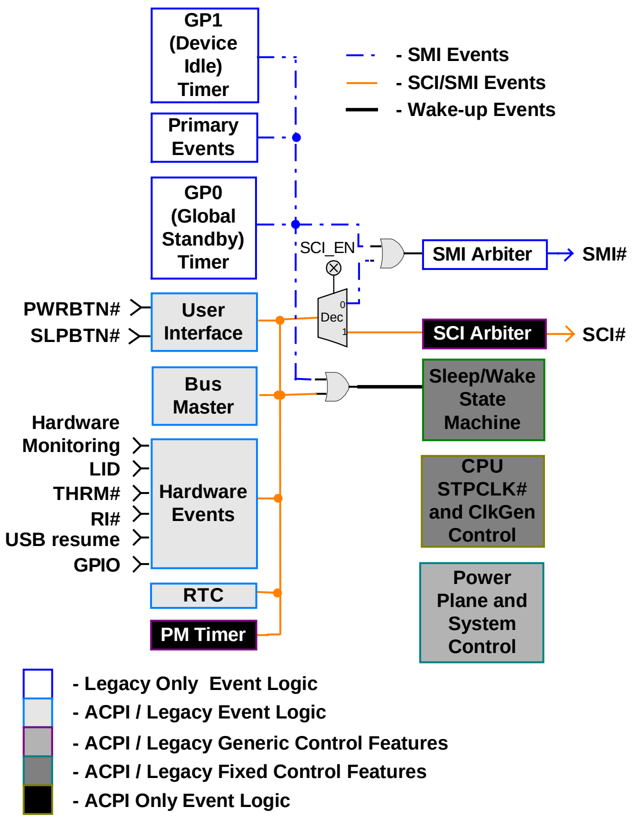


Figure 3. Power Management Subsystem Block Diagram

Refer to ACPI Specification v1.0 and APM specification v1.2 for additional information.

Processor Bus States

The VT8235 supports the complete set of C0 to C3 processor states as specified in the Advanced Configuration and Power Interface (ACPI) specification (and defined in ACPI I/O space Registers 10-15):

C0: Normal Operation

C1: CPU Halt (controlled by software).

C2: Stop Clock. Entered when the Processor Level 2 register (PMIO Rx14) is read. The STPCLK# signal is asserted to put the processor in the Stop Grant State. The CPUSTP# signal is not asserted so that host clocks remain running. To exit this state, the chip negates STPCLK#.

C3: Suspend. Entered when the Processor Level 3 register (PMIO Rx15) is read. In addition to STPCLK# assertion as in the C2 state, the SUSST1# (suspend status 1) signal is asserted to tell the north bridge to switch to “Suspend DRAM Refresh” mode based on the 32KHz suspend clock (SUSCLK) provided by the VT8235. If the Host Stop bit is enabled, then CPUSTP# is also asserted to stop clock generation and put the CPU into Stop Clock State. To exit this state, the chip negates CPUSTP# and allows time for the processor PLL to lock. Then the SUSST1# and STPCLK# signals are negated to resume to normal operation.

During normal operation, two mechanisms are provided to modulate CPU execution and control power consumption by throttling the duty cycle of STPCLK#:

a. Setting the Throttle Enable bit to 1, the duty cycle defined in Throttle Duty Cycle (PMIO Rx10) is used.
b. THRM# pin assertion enables automatic clock throttling with duty cycle pre-configured in THRM# Duty Cycle (PCI configuration Rx4C).

System Suspend States and Power Plane Control

There are three power planes inside the VT8235. The first power plane (VSUS33) is always on unless turned off by the mechanical switch. The second power plane (VCC) is controlled by chip output SUSC# (also called "PSON"). The third plane (VCCRTC) is powered by the combination of the VSUS33 and the external battery (VBAT) for the integrated real time clock. Most of the circuitry inside the VT8235 is powered by VCC. The amount of logic powered by VSUS33 is very small; its main function is to control the supply of VCC and other power planes. VCCRTC is always on unless both the mechanical switch and VBAT are removed.

The VT8235 supports multiple system suspend states by configuring the SLP_TYP field of ACPI I/O space register Rx4-5:

a) **POS (Power On Suspend):** Most devices in the system remain powered. The host bus is put into an equivalent of the C3 state. In particular, the CPU is put into the Stop Grant State or Stop Clock State depending on the setting of the Host Stop bit. SUSST1# is asserted to tell the north bridge to switch to "Suspend DRAM Refresh" mode based on the 32KHz SUSCLK provided by the VT8235. As to the PCI bus, setting the PCLK Run bit to 0 enables the CLKRUN protocol defined in the PCI Mobile Design Guide. That is, the PCKRUN# pin will be de-activated after the PCI bus is idle for 26 clocks. Any PCI bus masters including the north bridge may resume PCI clock operation by pulling the PCKRUN# pin low. During the PCKRUN# de-activation period, the PCISTP# pin may be activated to disable the output of the PCI clock generator if the PCI_STP bit is enabled. When the system resumes from POS, the VT8235 can optionally resume without resetting the system, can reset the processor only, or can reset the entire system. When no reset is performed, the chip only needs to wait for the clock synthesizer and processor PLL to lock before the system is resumed, which typically takes 20ms.

b) **STR (Suspend to RAM):** Power is removed from most of the system except the system DRAM. Power is supplied to the suspend refresh logic in the north bridge (e.g., VSUS25 of the VT8633) and the suspend logic of the VT8235 (VSUS33).

c) **STD (Suspend to Disk, also called Soft-off):** Power is removed from most of the system except the suspend logic of VT8235 (VSUS33).

d) **Mechanical Off:** This is not a suspend state. All power in the system is removed except the RTC battery.

The suspend state is entered by setting the Sleep Enable bit to 1. Three power plane control signals (SUSA#, SUSB# and SUSC#) are provided to turn off more system power planes as the system moves to deeper power-down states, i.e., from normal operation to POS (only SUSA# asserted), to STR (both SUSA# and SUSB# asserted), and to STD (all three SUS# signals asserted). In particular, the assertion of SUSC# can be used to turn off the VCC supply to the VT8235.

One additional suspend status indicator (SUSST1#) is provided to inform the north bridge and the rest of the system of the processor and system suspend states. SUSST1# is asserted when the system enters the suspend state or the processor enters the C3 state. SUSST1# is connected to the north bridge to switch between normal and suspend-DRAM-refresh modes.

General Purpose I/O Ports

As ACPI compliant hardware, the VT8235 includes PWRBTN#, SLPBTN#, and RI# pins to implement power button, sleep button, and ring indicator functionality, respectively. Furthermore, the VT8235 offers many general-purpose I/O ports with the following capabilities:

- **I^2C / SMB Support**
- **Thermal Detect**
- **Notebook Lid Open / Close Detect**
- **Battery Low Detect**
- **Twelve General Purpose Input Ports** (multiplexed with other functions).
- **Nineteen General Purpose Output Ports** (1 dedicated and 18 multiplexed with other functions)
- **Four General Purpose Input / Output Ports** (multiplexed with other functions)

In addition, the VT8235 provides an external dedicated SMI pin (EXTSMI#). The external SMI input can be programmed to trigger an SCI or SMI at both the rising and falling edges of the corresponding input signal. Software can check the status of the input pin and take appropriate actions.

Power Management Events

Three types of power management events are supported:

1) **ACPI-required Fixed Events** defined in the PM1a Status and PM1a Enable registers. These events can trigger either SCI or SMI depending on the SCI Enable bit:
   - PWRBTN# Triggering
   - RTC Alarm
   - Sleep Button
   - ACPI Power Management Timer Carry (always SCI)
   - BIOS Release (always SCI)

2) **ACPI-aware General Purpose Function Events** defined in the GP Status and GP SCI Enable, and GP SMI Enable registers. These events can trigger either SCI or SMI depending on the setting of individual SMI and SCI enable bits:
   - External SMI triggering
   - USB Resume
   - Ring Indicator (RI#)
   - Battery Low Detect (BATLOW#)
   - Notebook Lid Open/Close Detect (LID)
   - Thermal Detect (THRM#)

3) **Generic Global Events** defined in the Global Status and Global Enable registers. These registers are mainly used for SMI:
   - PCI Bus Clock Run Resume
   - Primary Interrupt Occurance
   - GP0 and GP1 Timer Time Out
   - Secondary Event Timer Time Out
   - Occurrence of Primary Events
     (defined in the Primary Activity Status and Primary Activity Enable registers)
   - Legacy USB accesses (keyboard and mouse)
   - Software SMI

System and Processor Resume Events

Depending on the system suspend state, different features can be enabled to resume the system. There are two classes of resume events:

a) VSUS-based events. Event logic resides in the VSUS plane and thus can resume the system from any suspend state. Such events include PWRBTN#, RI#, BATLOW#, LID, SMBus resume event, RTC alarm, EXTSMI#, and GP1 (EXTSMI1#).

b) VCC-Based Events. Event logic resides in the VCC plane and thus can only resume the system from the POS state. Such events include the ACPI PM timer, USB resume, and EXTSMIn#.

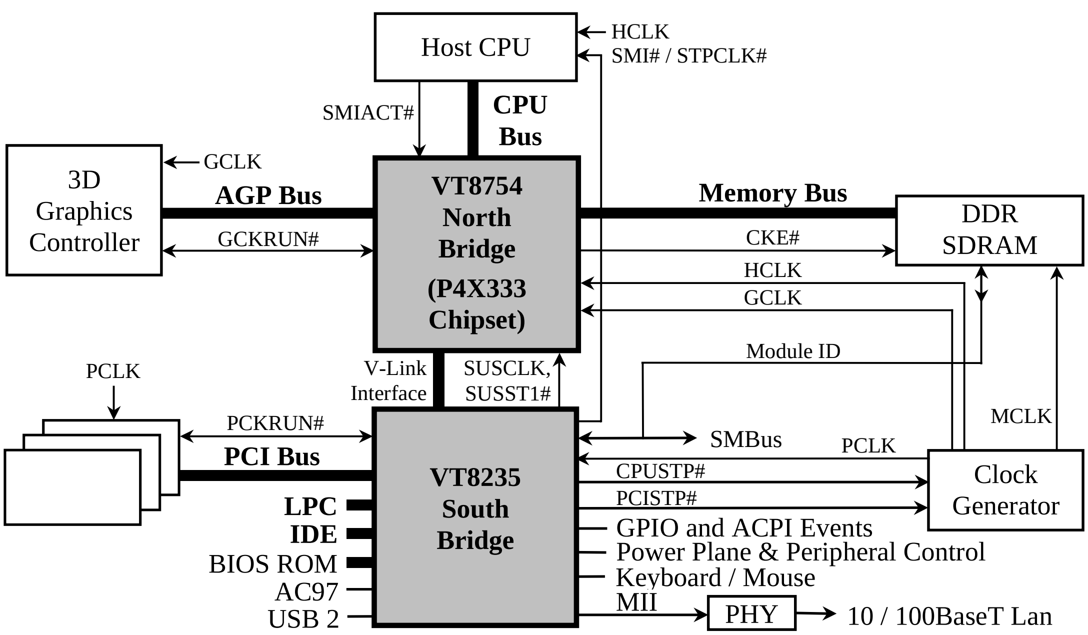


Figure 4. System Block Diagram Using the VT8754 North Bridge

Legacy Power Management Timers

In addition to the ACPI power management timer, the VT8235 includes the following four legacy power management timers:

GP0 Timer: general purpose timer with primary event

GP1 Timer: general purpose timer with peripheral event reload

Secondary Event Timer: to monitor secondary events

Conserve Mode Timer: Hardware-controlled return to standby

The normal sequence of operations for a general purpose timer (GP0 or GP1) is to

1) First program the time base and timer value of the initial count (register GP Timer Count).
2) Then activate counting by setting the GP0 Start or GP1 Start bit to one: the timer will start with the initial count and count down towards 0.
3) When the timer counts down to zero, an SMI will be generated if enabled (GP0 Timeout Enable and GP1 Timeout Enable in the Global Enable register) with status recorded (GP0 Tomeout Status and GP1 Timeout Status in the Global Status register).
4) Each timer can also be programmed to reload the initial count and restart counting automatically after counting down to 0. This feature is not used in standard VIA BIOS.

The GP0 and GP1 timers can be used just as the general purpose timers described above. However, they can also be programmed to reload the initial count by system primary events or peripheral events thus used as primary event (global standby) timer and peripheral timer, respectively. The secondary event timer is solely used to monitor secondary events.

System Primary and Secondary Events

Primary system events are distinguished in the Primary Activity Status and Primary Activity Enable registers:

Bit	Event	Trigger
7	**Keyboard Access**	I/O port 60h
6	**Serial Port Access**	I/O ports 3F8h-3FFh, 2F8h-2FFh, 3E8h-3EFh, or 2E8h-2EFh
5	**Parallel Port Access**	I/O ports 378h-37Fh or 278h-27Fh
4	**Video Access**	I/O ports 3B0h-3DFh or memory A/B segments
3	**IDE/Floppy Access**	I/O ports 1F0h-1F7h, 170h-177h, or 3F5h
2	**Reserved**	
1	**Primary Interrupts**	Each channel of the interrupt controller can be programmed to be a primary or secondary interrupt
0	**ISA Master/DMA Activity**	

Each category can be enabled as a primary event by setting the corresponding bit of the Primary Activity Enable register to 1. If enabled, the occurrence of the primary event reloads the GP0 timer if the Primary Activity GP0 Enable bit is also set to 1. The cause of the timer reload is recorded in the corresponding bit of Primary Activity Status register while the timer is reloaded. If no enabled primary event occurs during the count down, the GP0 timer will time out (count down to 0) and the system can be programmed (setting the GP0 Timeout Enable bit in the Global Enable register to one) to trigger an SMI to switch the system to a power down mode.

The VT8235 distinguishes two kinds of interrupt requests as far as power management is concerned: the primary and secondary interrupts. Like other primary events, the occurrence of a primary interrupt demands that the system be restored to full processing capability. Secondary interrupts, however, are typically used for housekeeping tasks in the background unnoticeable to the user. The VT8235 allows each channel of interrupt request to be declared as either primary, secondary, or ignorable in the Primary IRQ Channel and Secondary IRQ Channel registers. Secondary interrupts are the only system secondary events defined in the VT8235.

Like primary events, primary interrupts can be made to reload the GP0 timer by setting the PIRQ Enable bit to 1. Secondary interrupts do not reload the GP0 timer. Therefore the GP0 timer will time out and the SMI routine can put the system into power down mode if no events other than secondary interrupts are happening periodically in the background.

Primary events can be programmed to trigger an SMI (setting of the Primary Activity Enable bit). Typically, this SMI triggering is turned off during normal system operation to avoid degrading system performance. Triggering is turned on by the SMI routine before entering the power down mode so that the system may be returned to normal operation at the occurrence of primary events. At the same time, the GP0 timer is reloaded and the count down process is restarted.

Peripheral Events

Primary and secondary events define system events in general and the response is typically expressed in terms of system events. Individual peripheral events can also be monitored by the VT8235 through the GP1 timer. The following four categories of peripheral events are distinguished (via the GP Reload Enable register):

Bit-7 **Keyboard Access**
Bit-6 **Serial Port Access**
Bit-4 **Video Access**
Bit-3 **IDE/Floppy Access**

The four categories are subsets of the primary events as defined in Primary Activity Enable and the occurrence of these events can be checked through a common register Primary Activity Status. As a peripheral timer, GP1 can be used to monitor one (or more than one) of the above four device types by programming the corresponding bit to one and the other bits to zero. Time out of the GP1 timer indicates no activity of the corresponding device type and appropriate action can be taken as a result.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Comment
T_S	Storage Temperature	–55	125	ºC	
T_C	Case Operating Temperature	0	85	ºC	
V_{CC}	Core Voltage	–0.5	2.625	Volts	2.5V (VT8235L is 3.3V Core)
V_{SUS25}	Suspend Voltage – 2.5V	–0.5	V_{CC} + 0.3	Volts	2.5V
V_{SUSUSB}	Suspend Voltage – USB	–0.5	V_{CC} + 0.3	Volts	2.5V
V_{SUSMII}	Suspend Voltage – LAN	–0.5	V_{CC} + 0.3	Volts	2.5V
V_{CCVK}	V-Link Voltage	–0.5	V_{CC} + 0.3	Volts	2.5V
V_{CCPLL}	PLL Voltage	–0.5	V_{CC} + 0.3	Volts	2.5V
V_{CCUPLL}	USB PLL Voltage	–0.5	V_{CC} + 0.3	Volts	2.5V
V_{CCRAM}	RAM Voltage	–0.5	V_{CC} + 0.3	Volts	2.5V
V_{CC33}	I/O Voltage	–0.5	3.6	Volts	3.3V
V_{SUS33}	Suspend Voltage – 3.3V	–0.5	V_{CC33} + 0.3	Volts	3.3V
V_{CCUSB}	USB Voltage	–0.5	V_{CC33} + 0.3	Volts	3.3V
V_{CCMII}	LAN Voltage	–0.5	V_{CC33} + 0.3	Volts	3.3V
V_{BAT}	Battery Voltage	V_{CC33} – 0.9	V_{CC33} + 0.3	Volts	3.3V
V_{VLVREF}	Reference Voltage – V-Link	–0.5	V_{CCVK} * 0.38	Volts	0.9V
V_{PDVREF}	Reference Voltage – Primary IDE	–0.5		Volts	
V_{SDVREF}	Reference Voltage – Secondary IDE	–0.5		Volts	
	Input voltage (3.3V only inputs)	–0.5	V_{CC33} + 0.3	Volts	FERR#, USBCLK, PWRBTN#, EXTSMI#, BATLOW#, SMBCK1-2, SMBDT1-2

Note: Stress above the conditions listed may cause permanent damage to the device.
Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

T_C = 0 - 85°C

V_{CC} = V_{SUS25} = V_{SUSUSB} = V_{SUSMII} = V_{CCVK} = V_{CCPLL} = V_{CCUPLL} = V_{CCRAM} = 2.5V ±5%,

V_{CC33} = V_{SUS33} = V_{CCUSB} = V_{CCMII} = 3.3V ±5%, V_{BAT} = 3.3V +0.3 / –0.9V, V_{PDVREF} = V_{SDVREF} = V_{VLVREF} = 0.9V ±5%, GND = 0V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low voltage	–0.5	0.8	V	
V_{IH}	Input high voltage	2.0	V_{CC33} + 0.3	V	
V_{OL}	Output low voltage	–	0.45	V	I_{OL} = 4.0mA
V_{OH}	Output high voltage	2.4	–	V	I_{OH} = –1.0mA
I_{IL}	Input leakage current	–	±10	uA	$0 < V_{IN} < V_{CC33}$
I_{OZ}	Tristate leakage current	–	±20	uA	$0.45 < V_{OUT} < V_{CC33}$

Register Bits Powered by VBAT

Register	Description
RTC Rx0D[7]	VBAT Voltage OK
F0 Rx96[3:0]	CPU Frequency Strapping Value
PMIO Rx20[0]	GPI0 Status
PMIO Rx20[6]	INTRUDER# Status
PMIO Rx22[2]	Enable SCI on KBC PME Asserted

Register Bits Powered by VSUS25

Register	Description
F0 Rx81[2]	RTC Enable Gated During Soft Off
F0 Rx94[7:0]	Power Well Control Register
F0 Rx95[3:0]	Misc Power Well Control Register
PMIO Rx00[15,11,10,8]	Wake, Abnormal PowerOff, RTC Alarm, and Power Button Status bits
PMIO Rx02[10,8]	RTC Alarm and Power Button Enables
PMIO Rx04[12:10]	Sleep Type
PMIO Rx20[13,11,9:8,5:2]	AC97 Wakeup, LID, USB Resume, Ring, PME#, EXTSMI#, LAN PME, and KBC PME Status bits
PMIO Rx22[13,11,8,6:3,1:0]	SCI on corresponding bits of PMIO Rx20
PMIO Rx24[13,11,8,6:3,1:0]	SMI on corresponding bits of PMIO Rx20
PMIO Rx2C[7,5,2]	LID polarity, Battery Low Resume Disable, Power Button triggering select
PMIO Rx4C[4:0]	GPO 4:0 Output Value

Power Requirements

T_C = 0 - 85°C

V_{CC} = V_{SUS25} = V_{SUSUSB} = V_{SUSMII} = V_{CCVK} = V_{CCPLL} = V_{CCUPLL} = V_{CCRAM} = 2.5V ±5%,

V_{CC33} = V_{SUS33} = V_{CCUSB} = V_{CCMII} = 3.3V ±5%, V_{BAT} = 3.3V +0.3 / –0.9V, V_{PDVREF} = V_{SDVREF} = V_{VLVREF} = 0.9V ±5%, GND = 0V

Symbol	Parameter	Typ	Max	Unit	Condition
I_{CC}	Power Supply Current – Core (3.3V)			mA	At max operating frequency
I_{CC33}	Power Supply Current – I/O (3.3V)			mA	At max operating frequency
I_{SUS33}	Power Supply Current – Suspend (3.3V)			mA	At max operating frequency
I_{SUS25}	Power Supply Current – Suspend (2.5V)			mA	At max operating frequency
I_{SUSUSB}	Power Supply Current – Suspend USB (2.5V)			mA	At max operating frequency
I_{SUSMII}	Power Supply Current – Suspend LAN (2.5V)			mA	At max operating frequency
I_{CCUSB}	Power Supply Current – USB (3.3V)			mA	At max operating frequency
I_{CCUPLL}	Power Supply Current – USB PLL (2.5V)			mA	At max operating frequency
I_{CCPLL}	Power Supply Current – PLL (2.5V)			mA	At max operating frequency
I_{CCVK}	Power Supply Current – V-Link (2.5V)			mA	At max operating frequency
I_{CCMII}	Power Supply Current – LAN (3.3V)			mA	At max operating frequency
I_{CCRAM}	Power Supply Current – RAM (2.5V)			mA	At max operating frequency
I_{VLVREF}	Power Supply Current – V-Link Reference (0.9V)			**uA**	At max operating frequency
I_{PDVREF}	Power Supply Current – Primary IDE Reference			**uA**	At max operating frequency
I_{SDVREF}	Power Supply Current – Secondary IDE Reference			**uA**	At max operating frequency
I_{BAT}	Power Supply Current – RTC Battery (3.3V)		5	**uA**	At max operating frequency
P_D	Power Dissipation		2.5	W	At max operating frequency

PACKAGE MECHANICAL SPECIFICATIONS

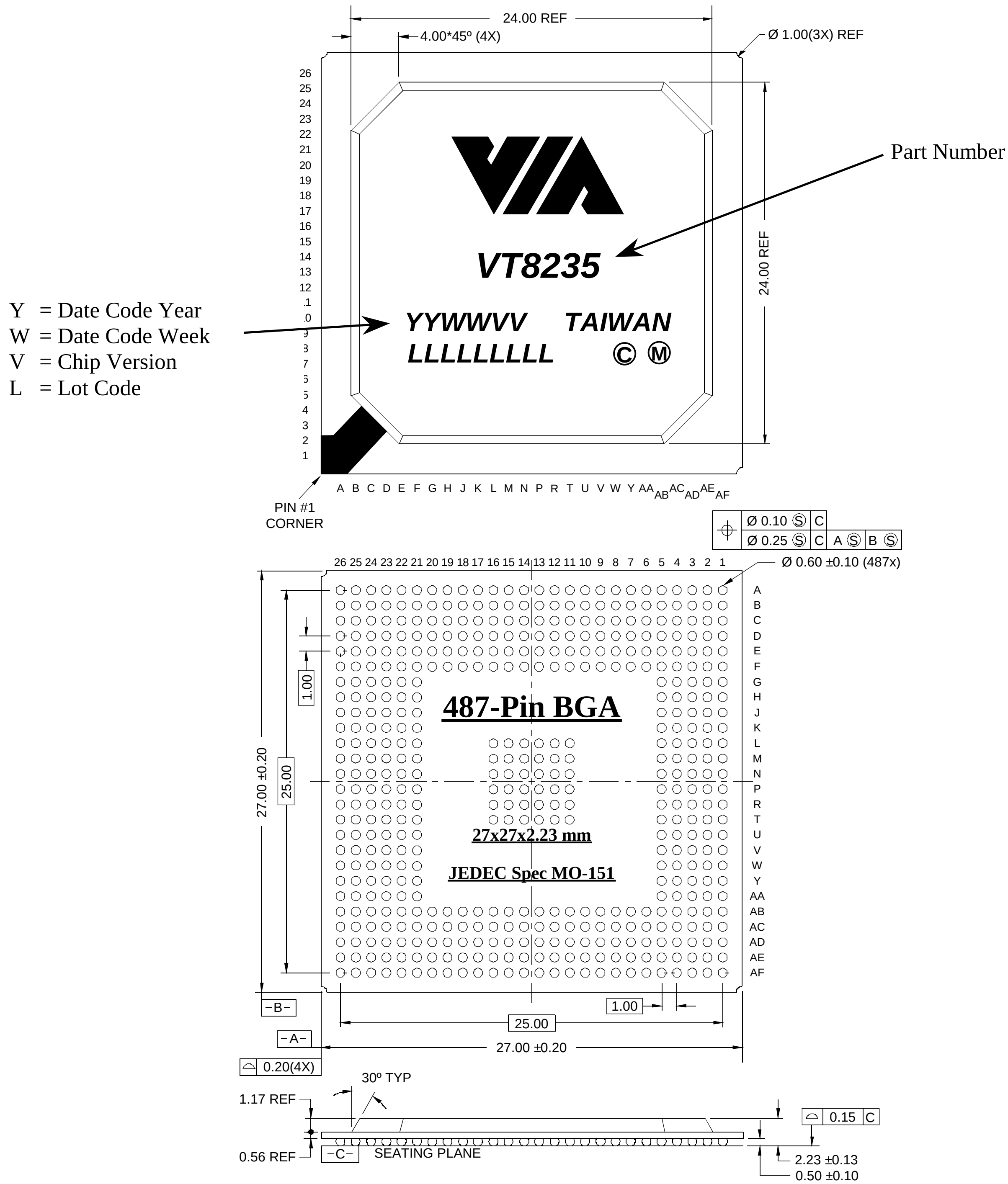


Figure 5. Mechanical Specifications – 487 Pin Ball Grid Array Package